Transistors

Semiconductors

Impurities in the semiconductor material makes it a wonder material also called doping

n-type, donor - electrons as a majority carrier

p-type, acceptor - holes as a majority carrier

Diodes

Combination of two material *p*-type and *n*-type

Forward biased - like a conductor, majority carrier is the conductor, low resistance

Reverse biased - like a very high resistance, minority carrier is the conductor

Works as a one-way flow control

Transistors

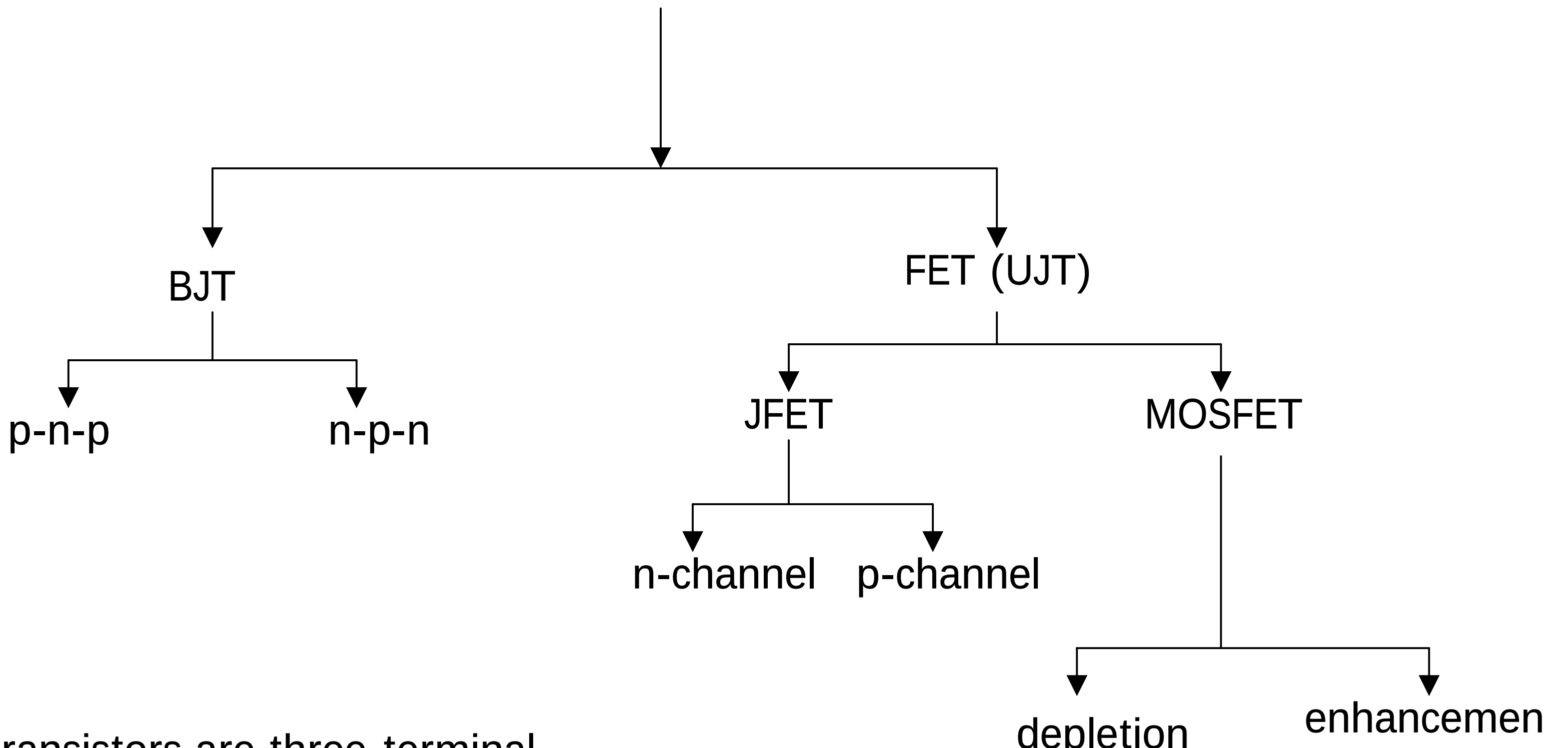
- It's a three layer (terminal) semiconductor device
- Two *n* and one *p* type or two *p* and one *n* type layers
- Two *n* and one *p* type is *npn transistor*
- Two *p* and one *n* type is *pnp transistor*

- *Two types*-
  - *Bipolar junction transistor(BJT)*

    Both electrons and holes participate in current flow
  - *Unipolar junction transistor(UJT)*

    Only one, either electrons or holes participate in current flow

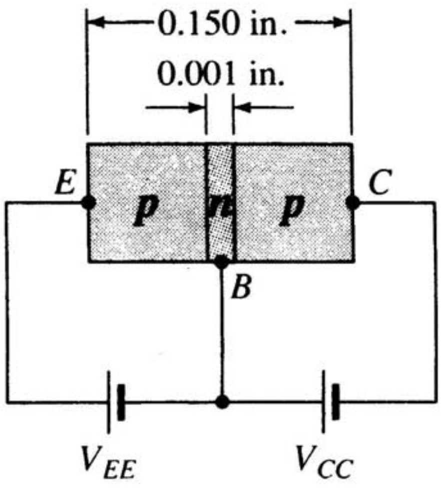
Transistor family



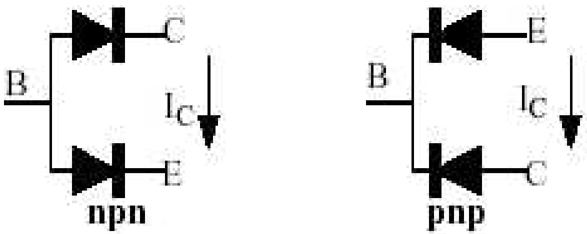
Transistors are three-terminal semiconductor devices

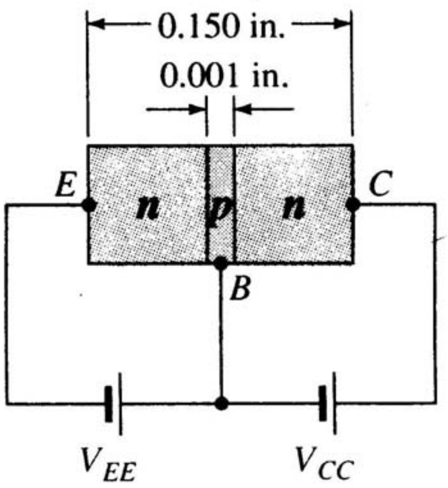
Transistors

- Three terminals - Emitter, base, collector
- Middle layer or sandwich layer
  - thin compare to outer layers
  - lightly doped, less free carriers
- Can be considered as two diodes connected back to back



(a)





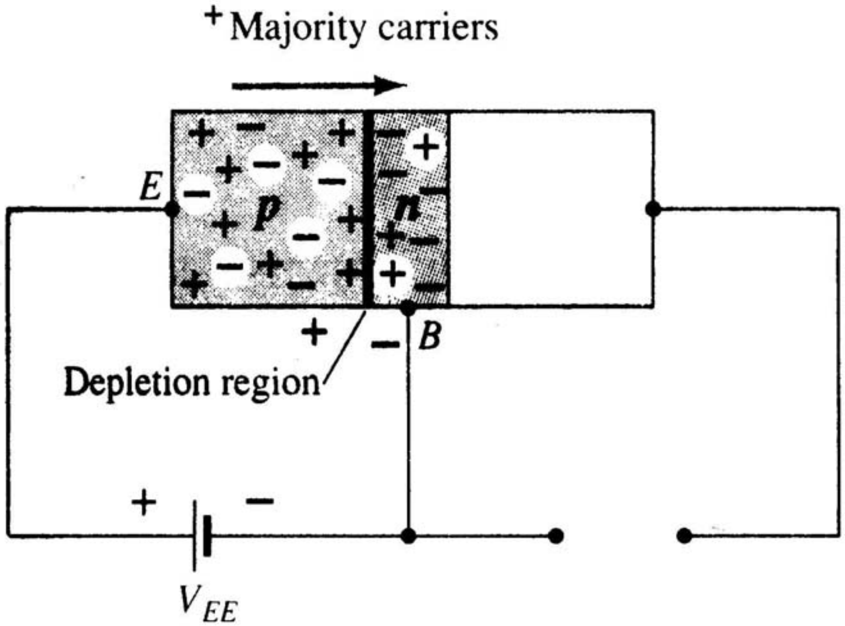
(b)

Transistor operation

Forward biased diode - *pn* junction, emitter-base

Base- collector is open circuit.

Depletion layer is reduced and behave like a normal diode

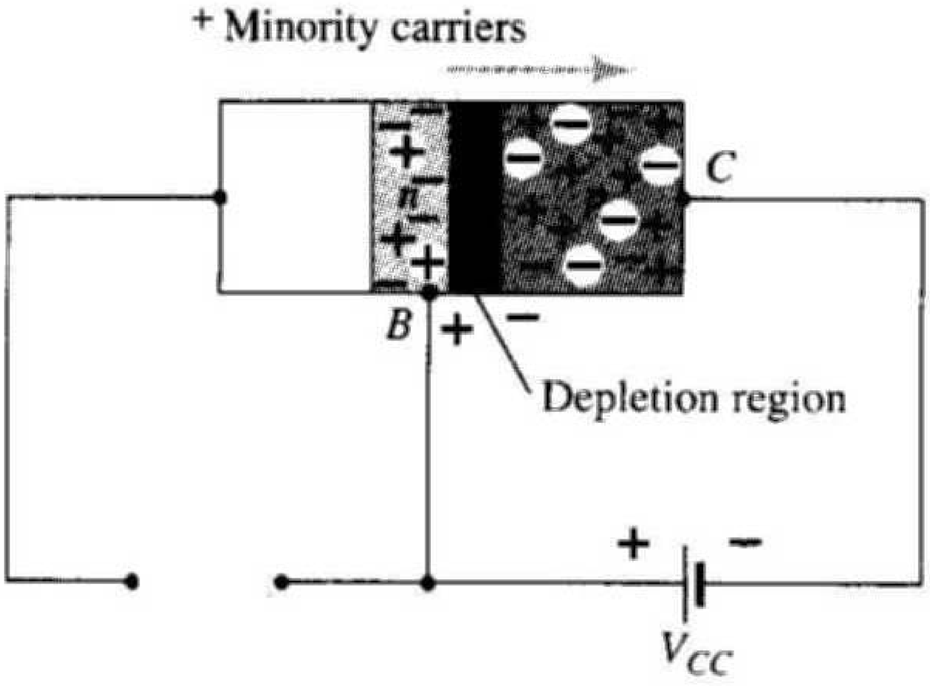


Forward biased junction of a *pnp* transistor

Transistor operation

Reverse biased diode - *np* junction, base collector

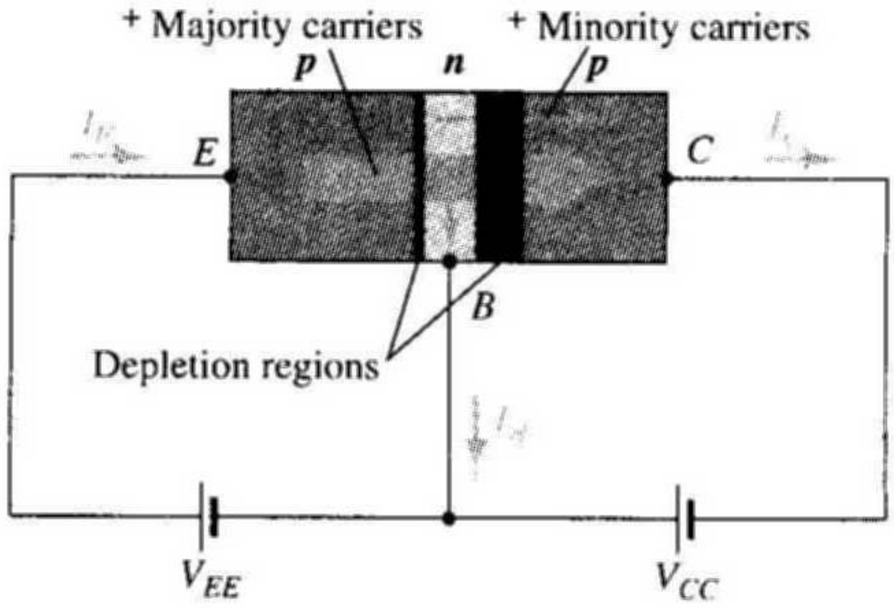
Depletion layer is increased and behave like a reverse biased diode



Transistor operation

Forward biased emitter-base, and reverse biased base collector

Base is lightly doped, unable to handle large majority carriers. Diffuse to collector which is reverse bias, ready to accept the diffused holes.



Modes of transistor operation

- Common - base
- Common - emitter
- Common - collector

Particular terminal is common to both input and output

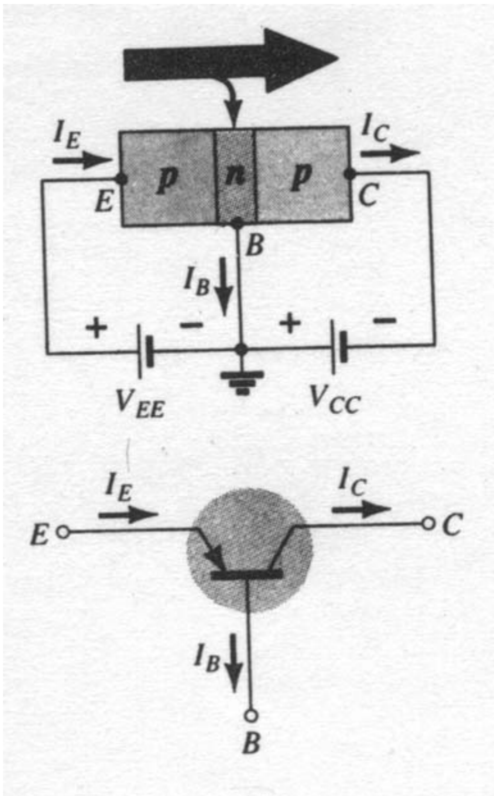
BJT Transistors

The arrow on the emitter lead shows the direction of current flow, when emitter-base junction is forward biased, it is always from *p to n*

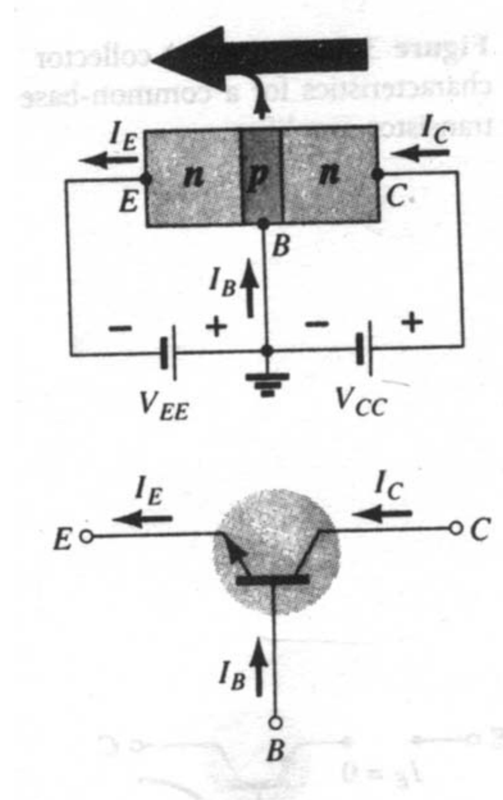
Currents are positive when flows inside the transistors

For a *pnp* transistor it will be inward and for *npn* transistor it will be outward

Common - base



(a)



(b)

pnp transistor

npn transistor

Current direction changes in the above two configuration

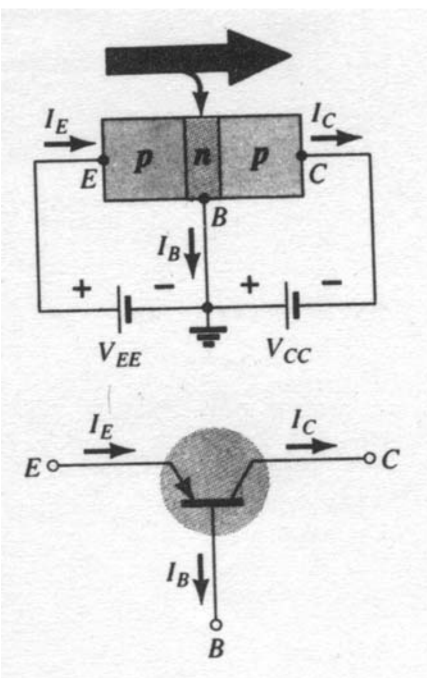
Common - base

Base is common to input and output

Emitter-base junction is forward biased

Collector-base junction is reverse biased

Biasing remains same irrespective of *npn* or *pnp*

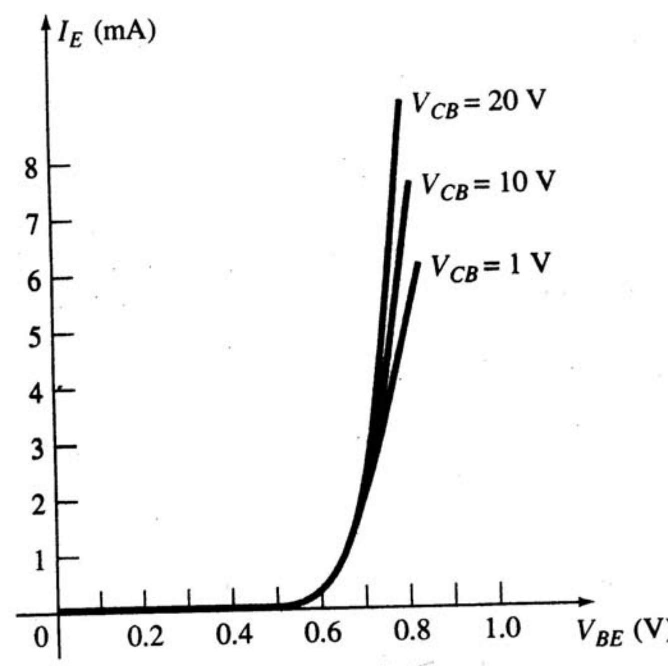


(a)

Input characteristics for a common base silicon transistor

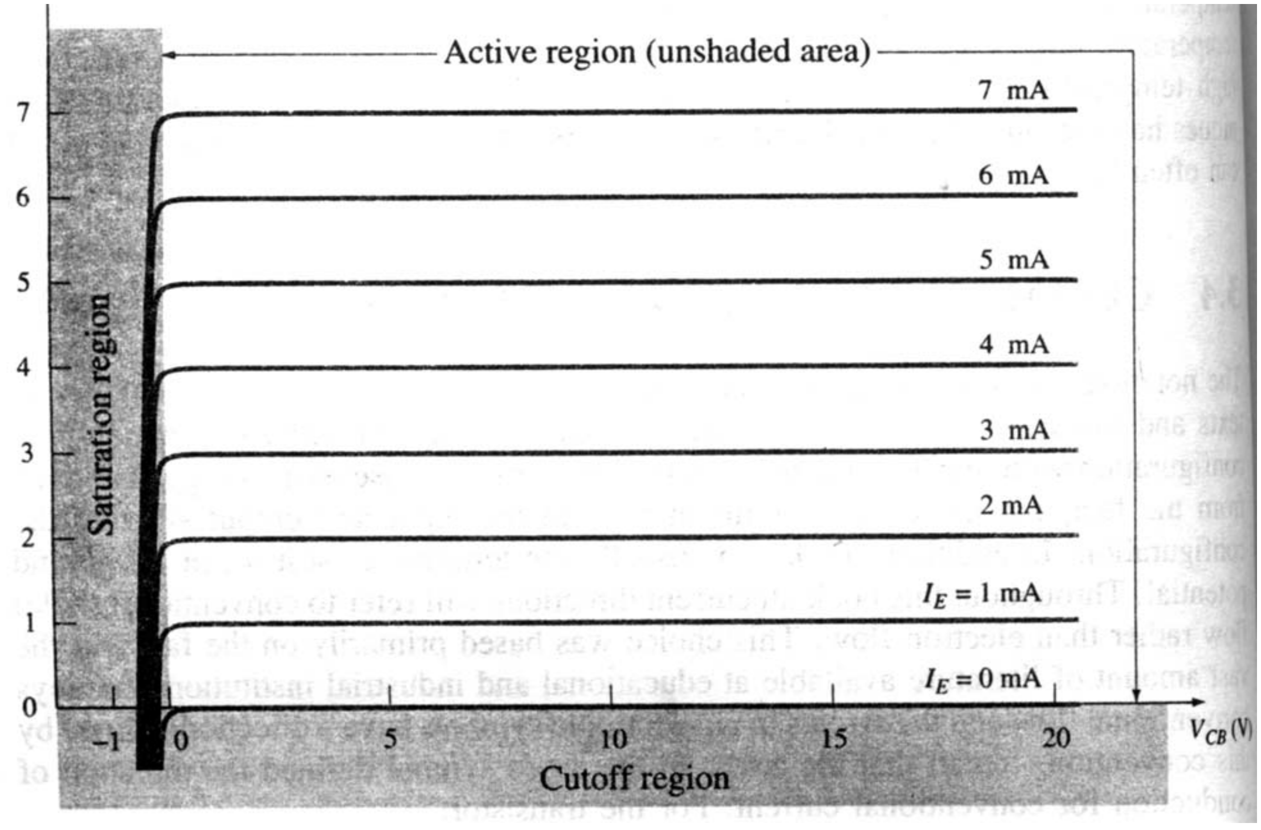
-like a *pn* junction

- V_{CB} not having major influence



Common - base

Active region - base-emitter forward biased and collector-base is reverse biased



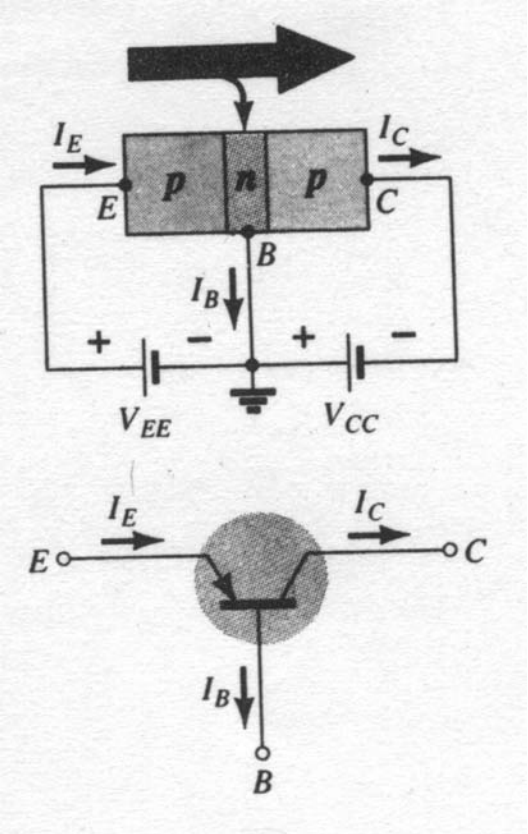
Common - base

$I_E = I_B + I_C$

Current in base is negligible.
Current in emitter and collector is almost same.

Current gain less than unity

$\alpha = I_C/I_E$ (0.90 - 0.998)



(a)

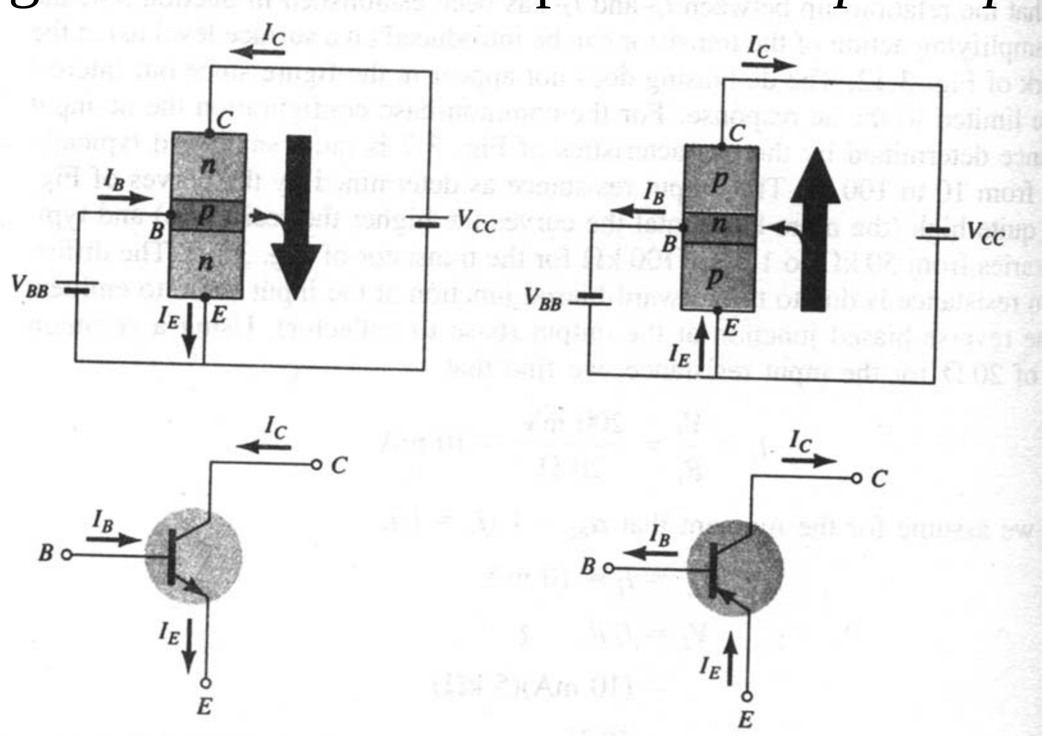
Common - emitter

Emitter is common to input and output

Base-emitter junction is forward biased

Collector-emitter junction is reverse biased

Biasing remains same irrespective of *npn* or *pnp*

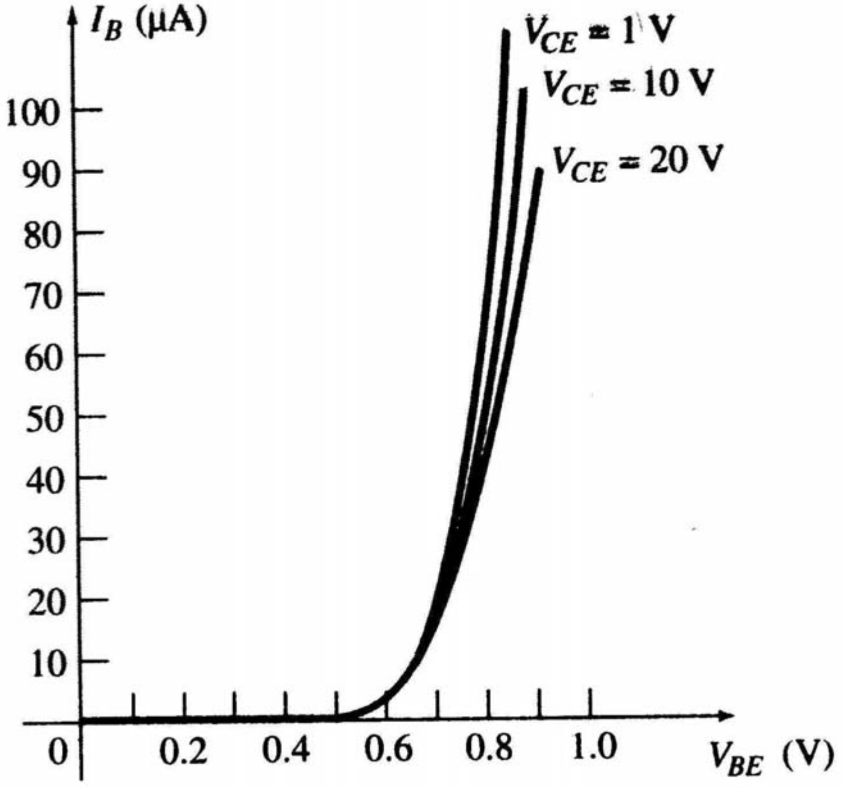


Common - emitter

Base-emitter *pn* junction, forward biased

Base current is in micro ampere

V_{CE} does not have major influence on I_B



(b)

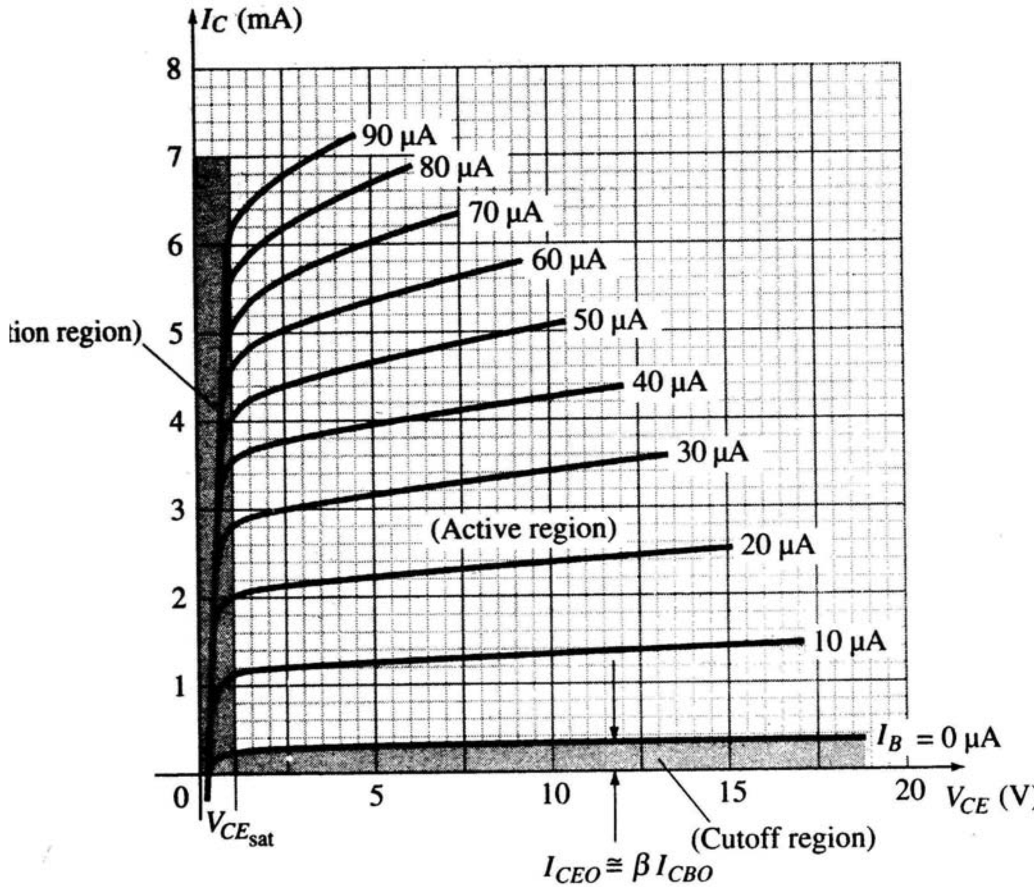
Common - emitter

Base-emitter *pn* junction, forward biased & base collector is reverse biased.

Base current is in micro ampere, collector current in milli ampere

High current gain

Cutoff region below $I_B = 0$



(a)

Common - emitter

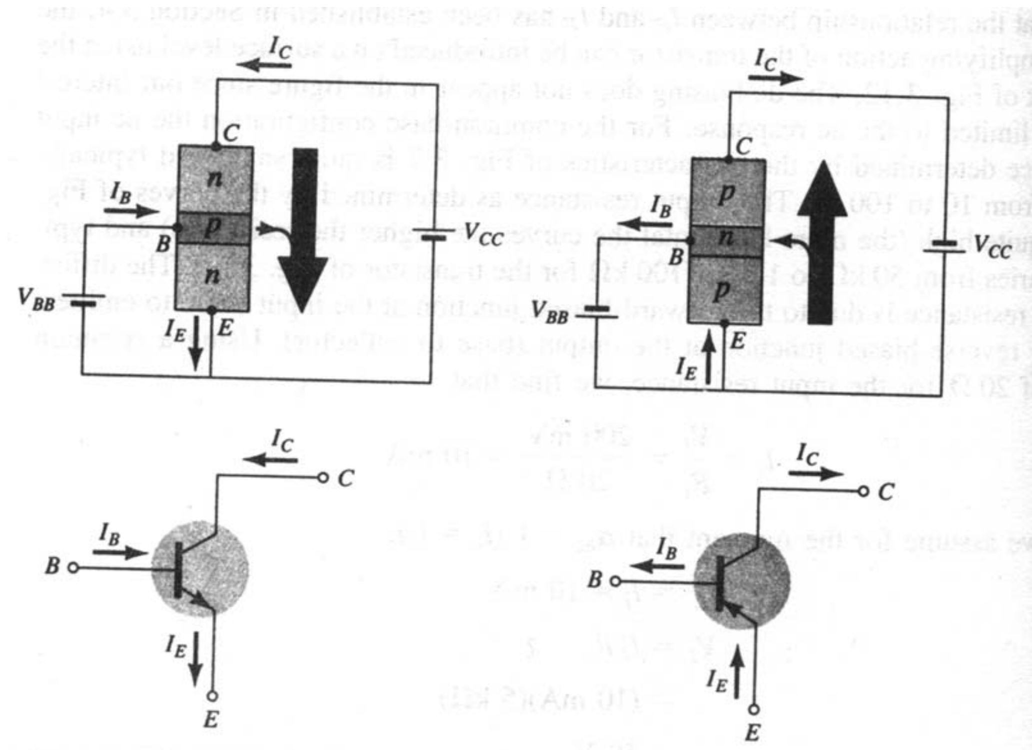
$I_C = \alpha I_E + I_{CBO}$

I_{CBO} current collector to base when emitter is open, minority current

$I_E = I_B + I_C$

$I_C = \alpha (I_B + I_C) + I_{CBO}$

$$I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$



Current Gain $\beta = I_C/I_B$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{1+\beta}$$

$\beta = (50 - 250)$

Common - collector

Collector is common to input and output

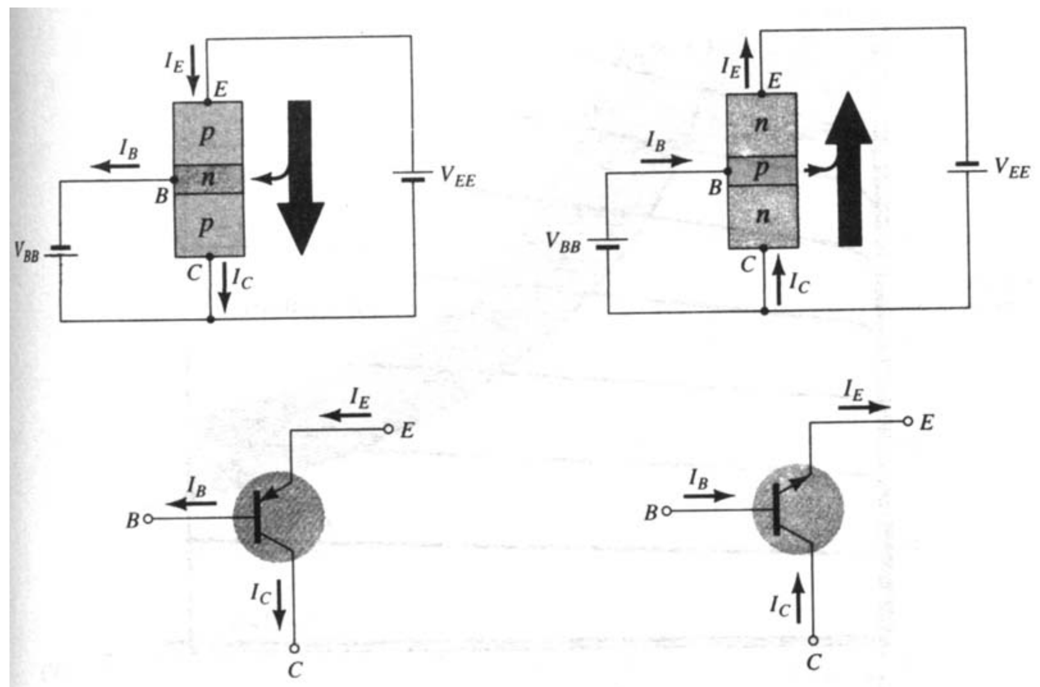
Base-collector junction is forward biased

Base-emitter junction is reverse biased

Biasing remains same irrespective of *npn* or *pnp*

Characteristics same as common emitter

Input resistance is very high and output resistance is low.

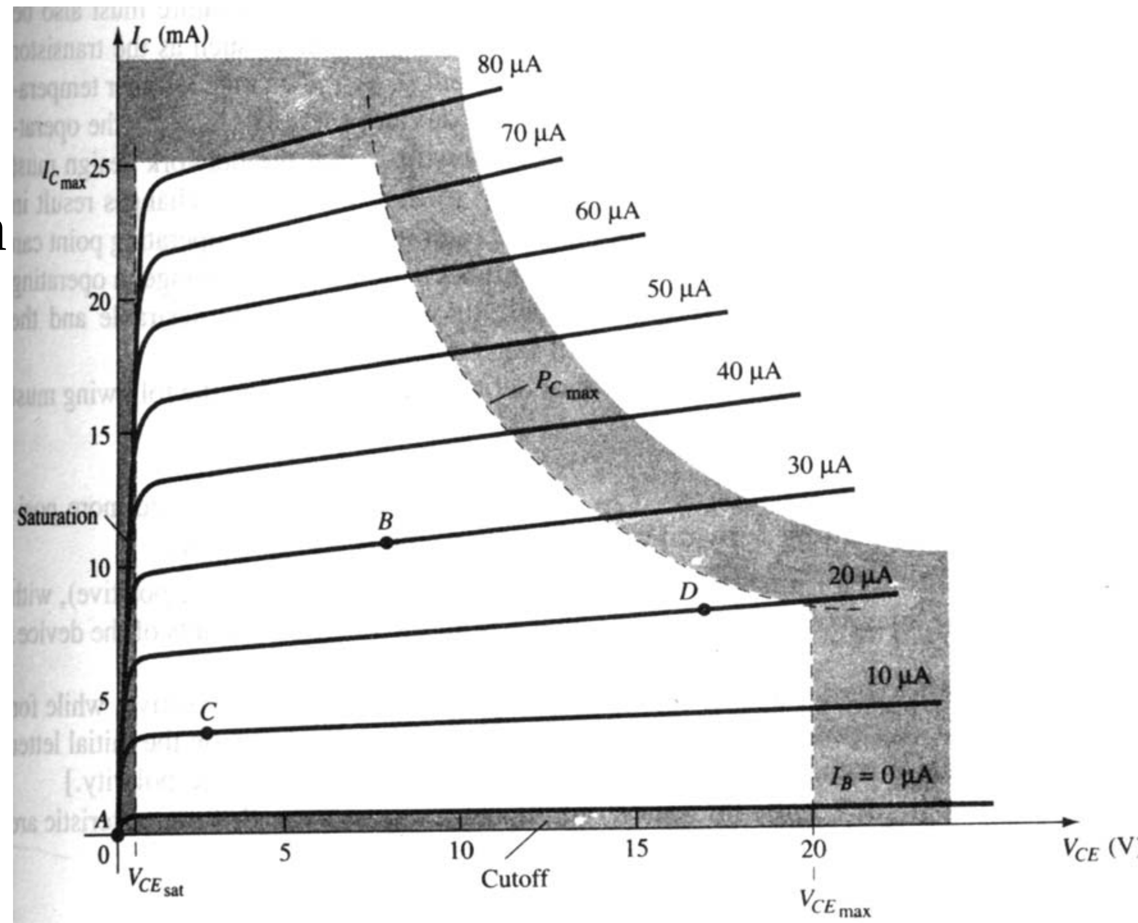


(a)
(b)

DC Biasing - BJT

Biasing - shifting the mean operating point. To avoid operation in

- Non-linear region
- Saturation region
- Cut-off region
- Max. power consumption



Linear region operation

Base-emitter forward bias

Base-collector reverse bias

Cutoff region

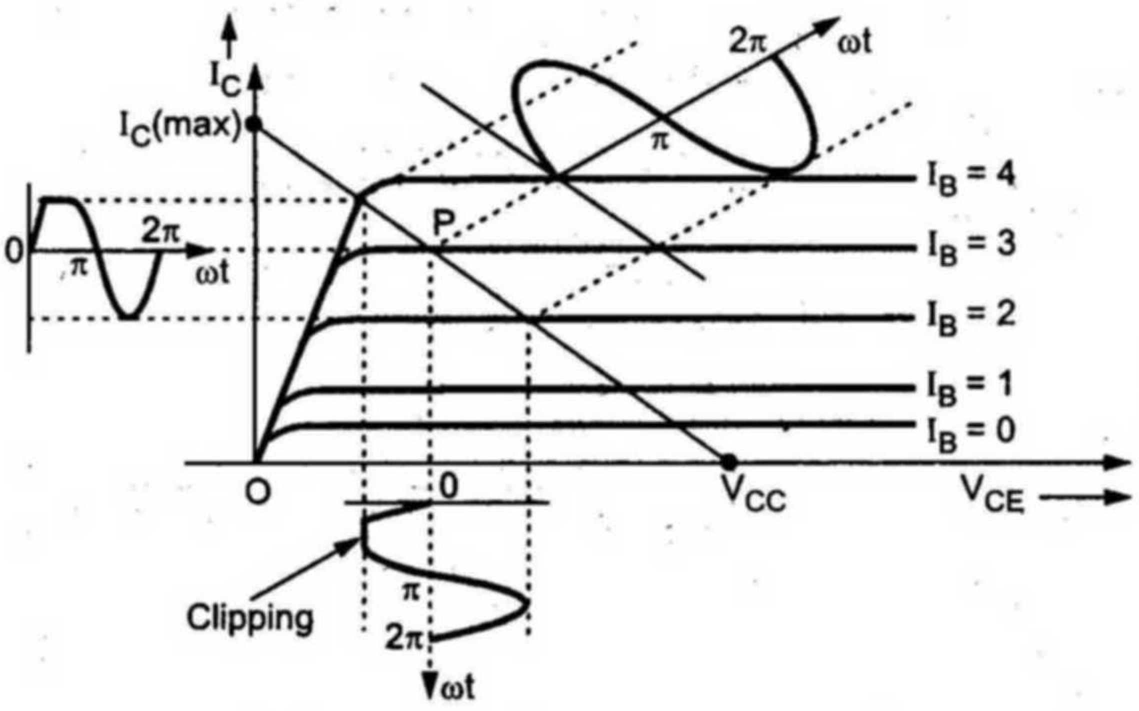
Base-emitter reverse bias

Saturation region

Base-emitter forward bias

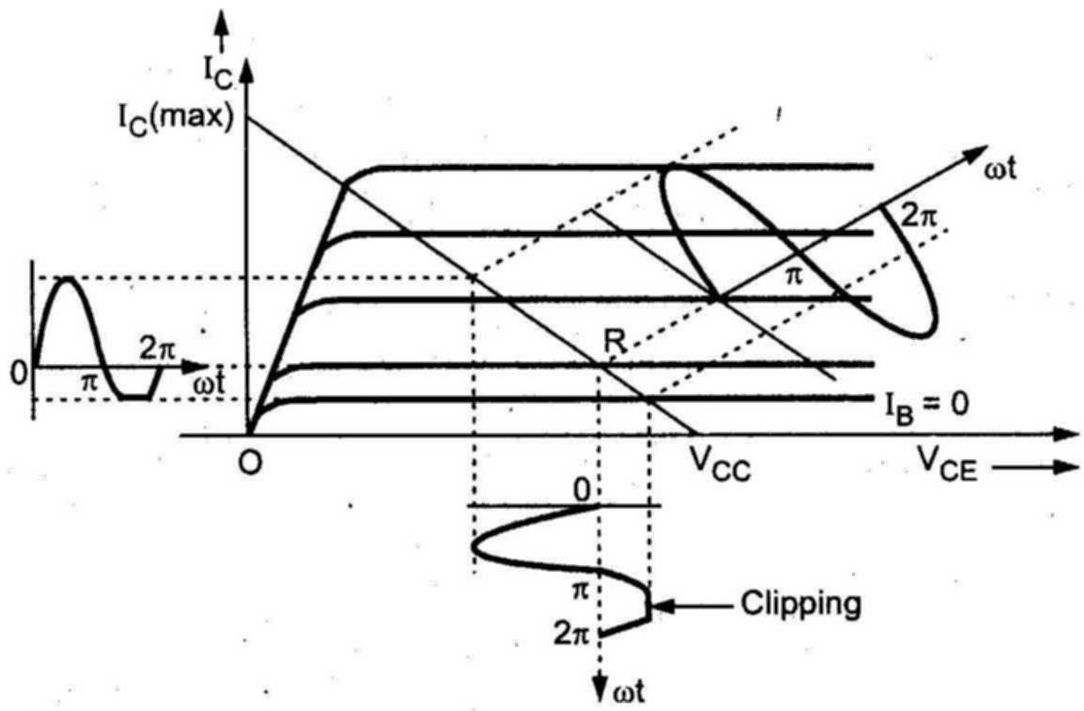
Base-collector forward bias

DC Biasing - BJT



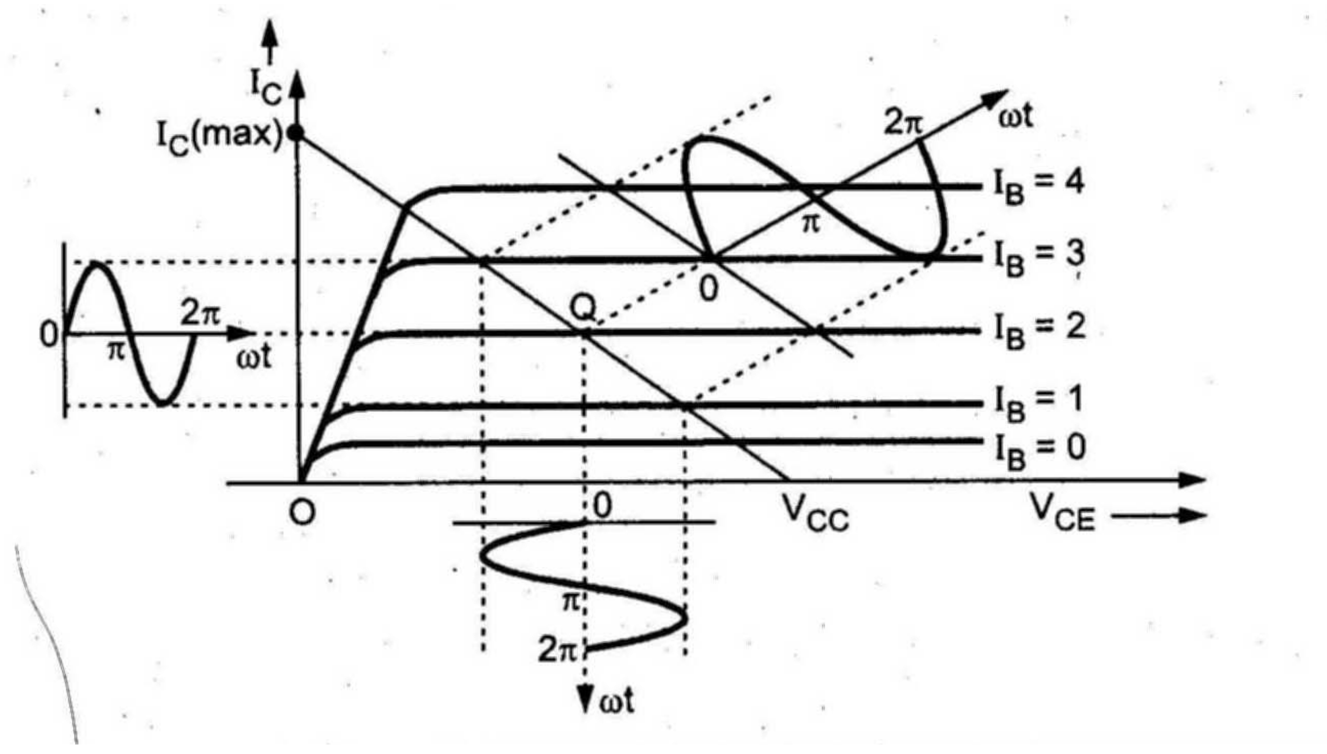
Clipping due to saturation region, base-collector junction gets forward biased

DC Biasing - BJT



Clipping due to cutoff region.

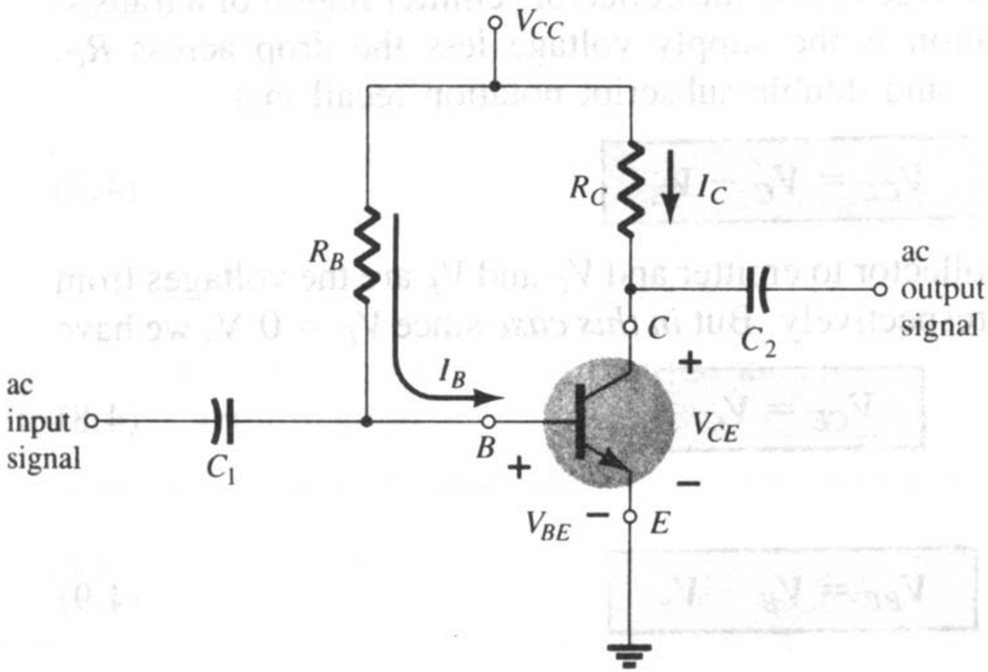
DC Biasing - BJT



Chosen Quiescent point is good for the given input signal

Fixed Bias Circuit

Biasing is decided by the resistance R_B and R_C connected to base and collector. These decide the mean operating point. For DC analysis, circuit without capacitor can be analysed.



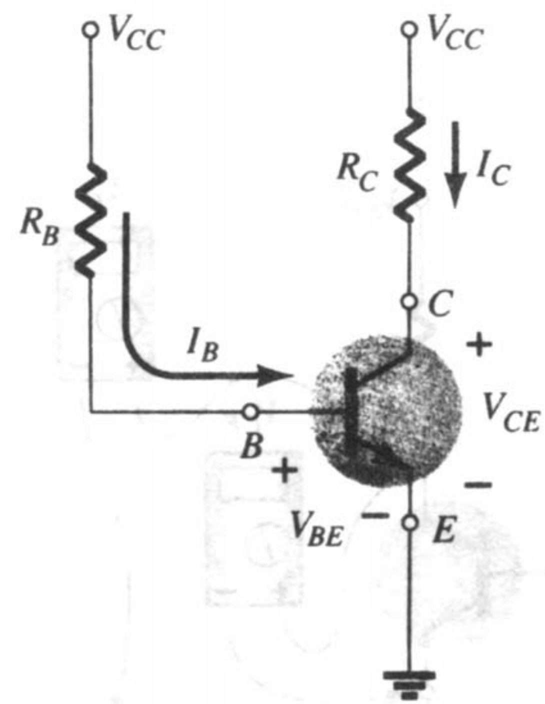


Figure 4.3 Dc equivalent of Fig. 4.2.

Fixed Bias Circuit

Base-emitter loop

$+V_{CC} - I_B R_B - V_{BE} = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

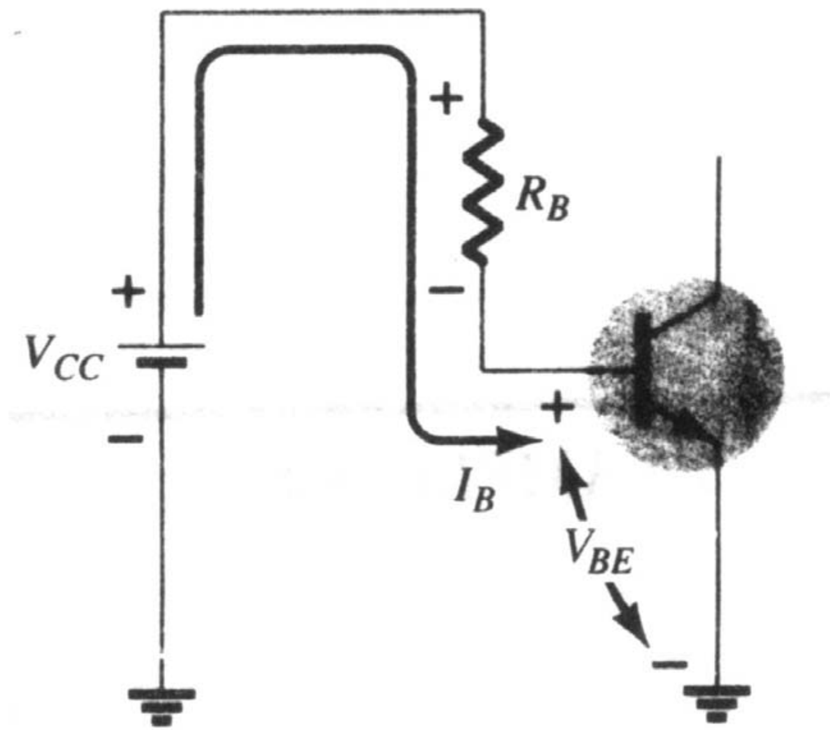


Figure 4.4 Base–emitter loop.

Fixed Bias Circuit

Collector-emitter loop

$I_C = \beta I_B$

$V_{CE} + I_C R_C - V_{CC} = 0$

$V_{CE} = V_{CC} - I_C R_C$

$V_{CE} = V_C - V_E$

$V_{BE} = V_B - V_E$

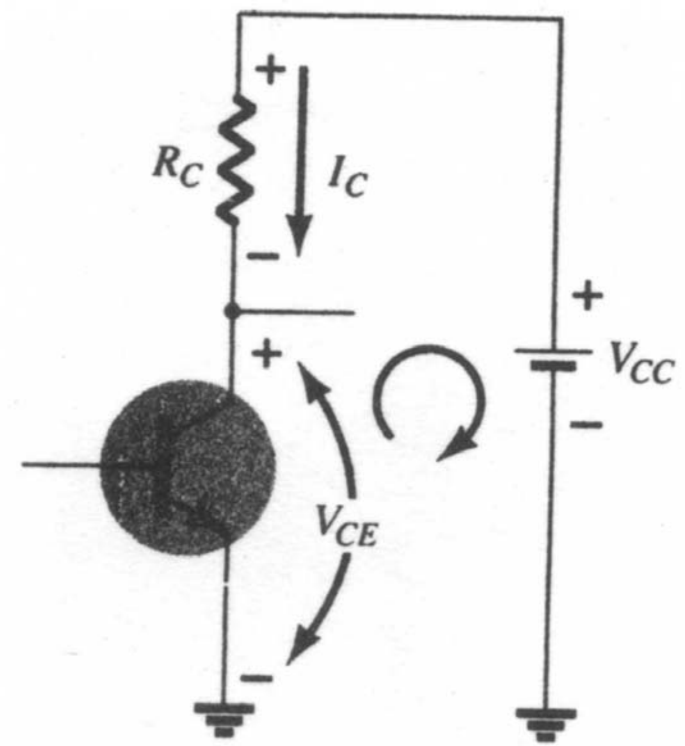
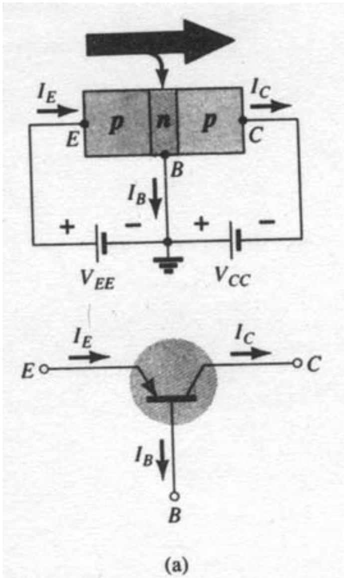
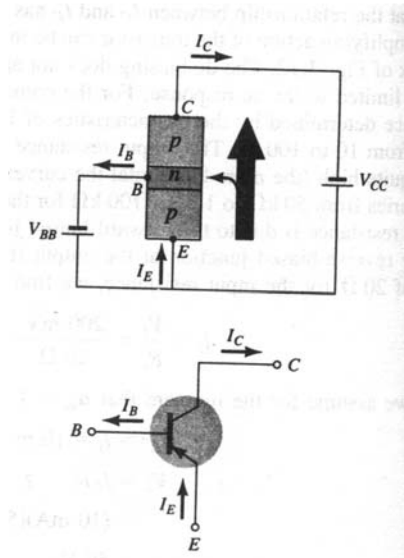
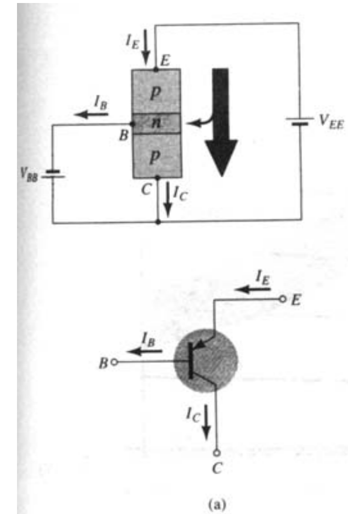


Figure 4.5 Collector–emitter loop.

BJT







Common base Common emitter Common collector

Common emitter has a good voltage gain

Common base, good voltage gain, disadvantage of low input impedance

Common collector, voltage gain ~ 1, high input impedance and low output impedance. Good for impedance matching

Unipolar Junction Transistors

Unipolar device solely depends on electron (*n*-channel) or hole (*p*-channel) conduction. Three terminal device.

Field Effect Transistor (FET) is a Unipolar device

Conduction is controlled by the electric field. No need of direct contact between the controlling and controlled quantities

JFET - Junction Field Effect Transistor

MOSFET - Metal Oxide Semiconductor FET

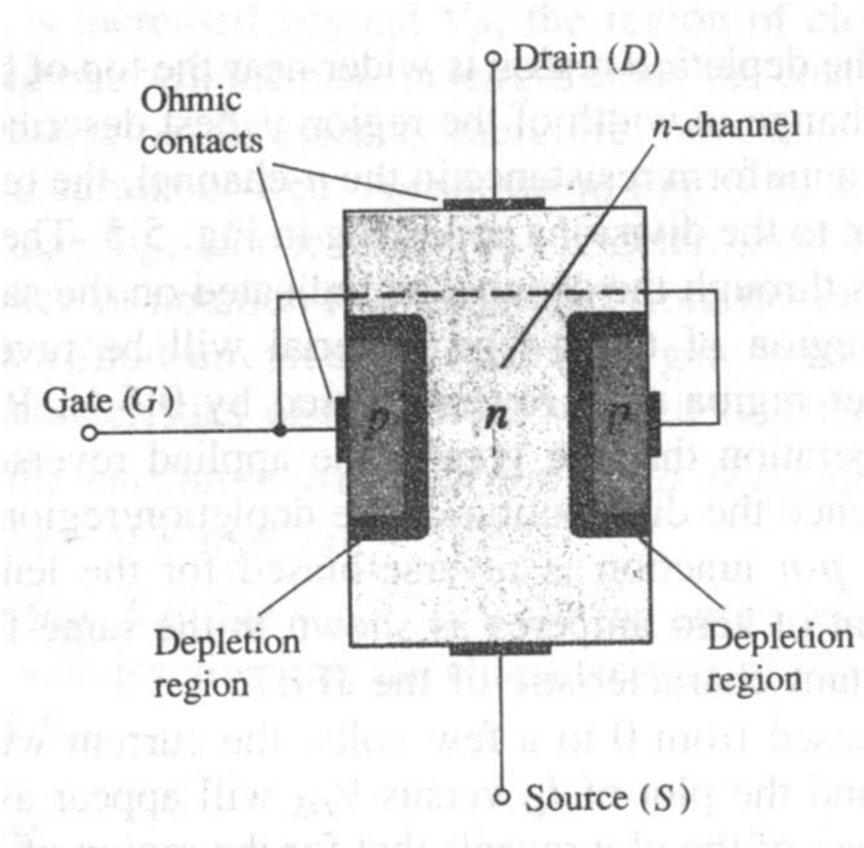
Junction Field Effect Transistors - JFET

Major part is *n*-type material channel, embedded between two *p*-type material.

Two ends of the *n*- type material channel are Drain (D) and source (S)

Two *p*-type material are connected together and referred as Gate (G)

Two *pn* junctions, depletion region at each junction



Junction Field Effect Transistors - JFET

V_{GS} = 0 v and V_{DS} some positive value

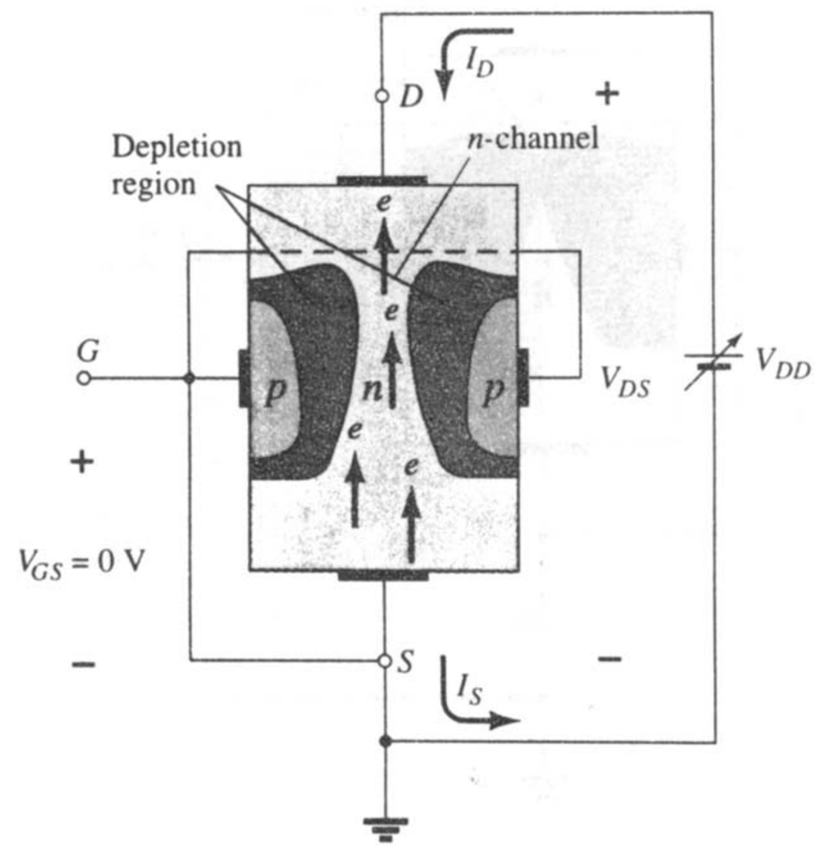
Gate and Source are same potential

Electrons will flow from source to drain as in *n* type semiconductor

$I_D = I_S$

Resistance of *n*-channel acts between drain and source

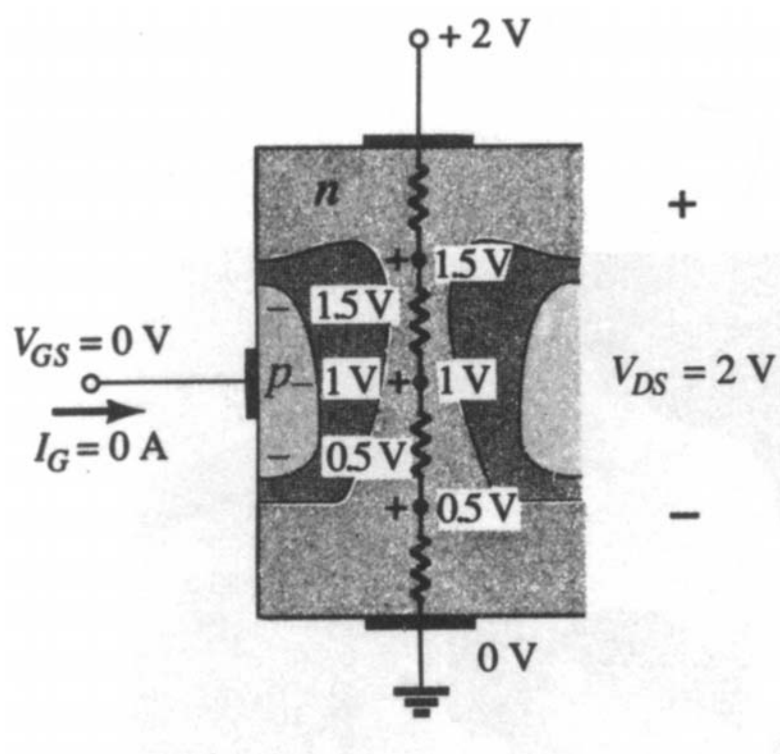
Depletion region is wider near the top of *p*-region



Junction Field Effect Transistors - JFET

Resistance of *n*-channel is uniform along the length. This works as a potential divider.

This leads to a variable reverse bias along the length. Maximum at top of *p*-material Reverse bias will depend on the current in *n*-channel. More the current more the potential drop



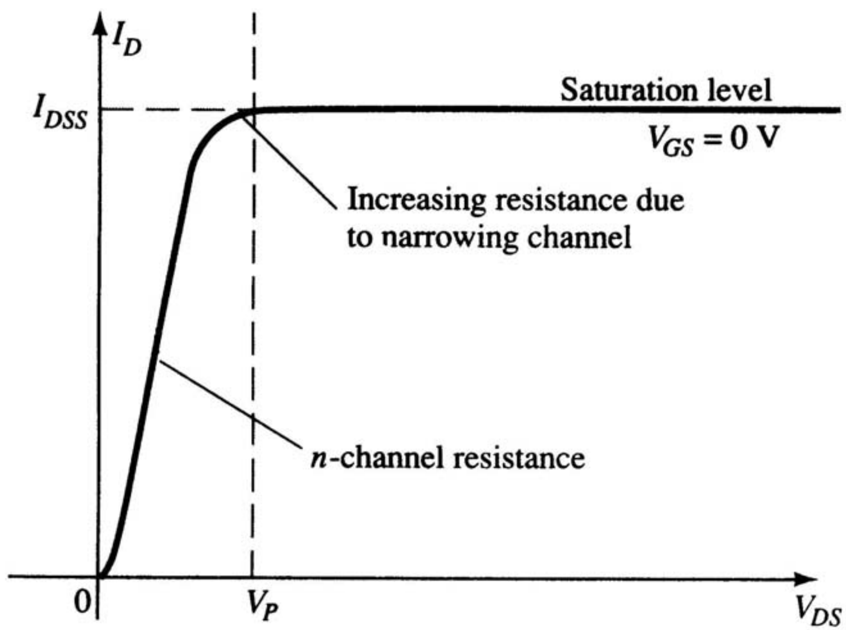
Junction Field Effect Transistors - JFET

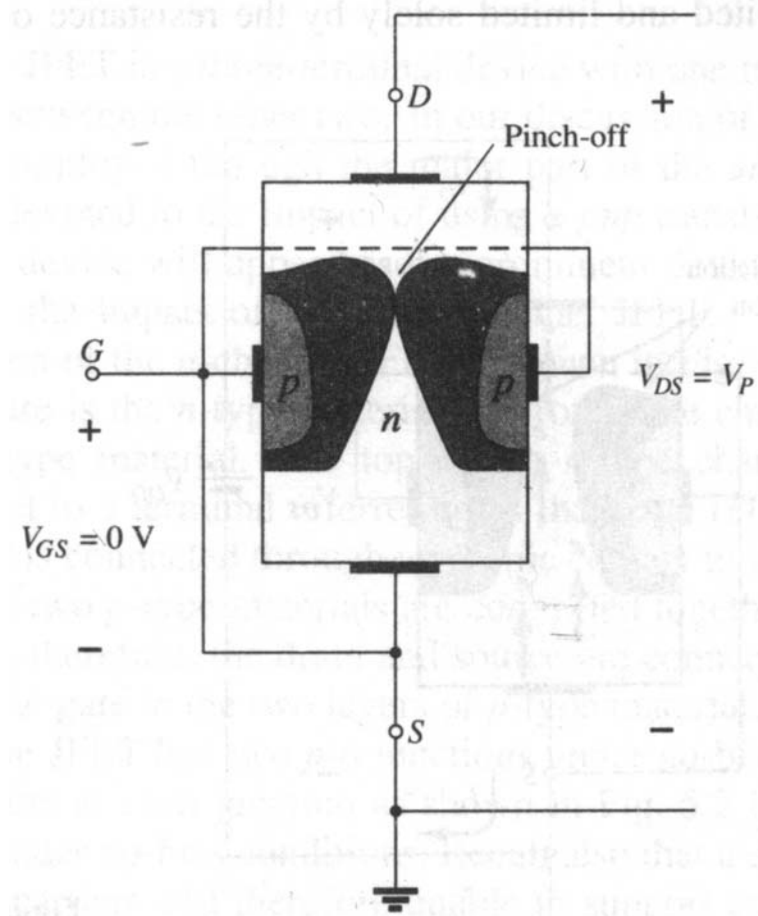
Initially it follows Ohm's law (almost straight line)

Later depletion layer widens

Pinch off level - depletion layer cannot increase more (very high resistance)

Give a feeling I_D will be zero. This is not possible



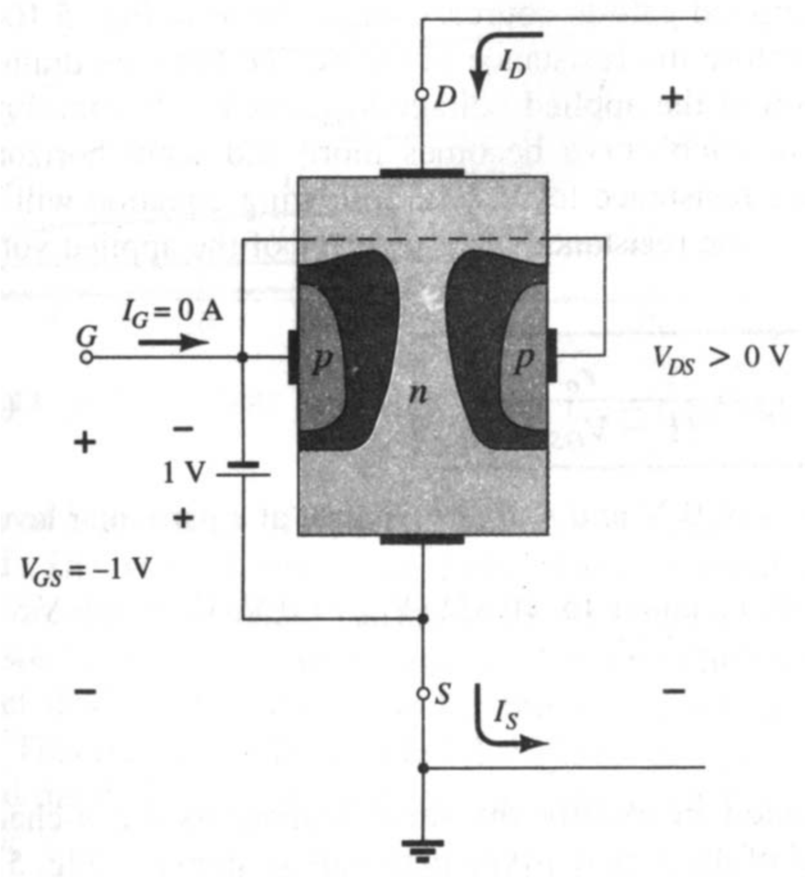


Junction Field Effect Transistors - JFET

V_{GS} < 0 v and V_{DS} some positive value

Gate to source voltage non zero

V_{GS} < 0 v more reverse bias and hence reduces saturation level for I_D. This will further reduce with reduction in V_{GS}

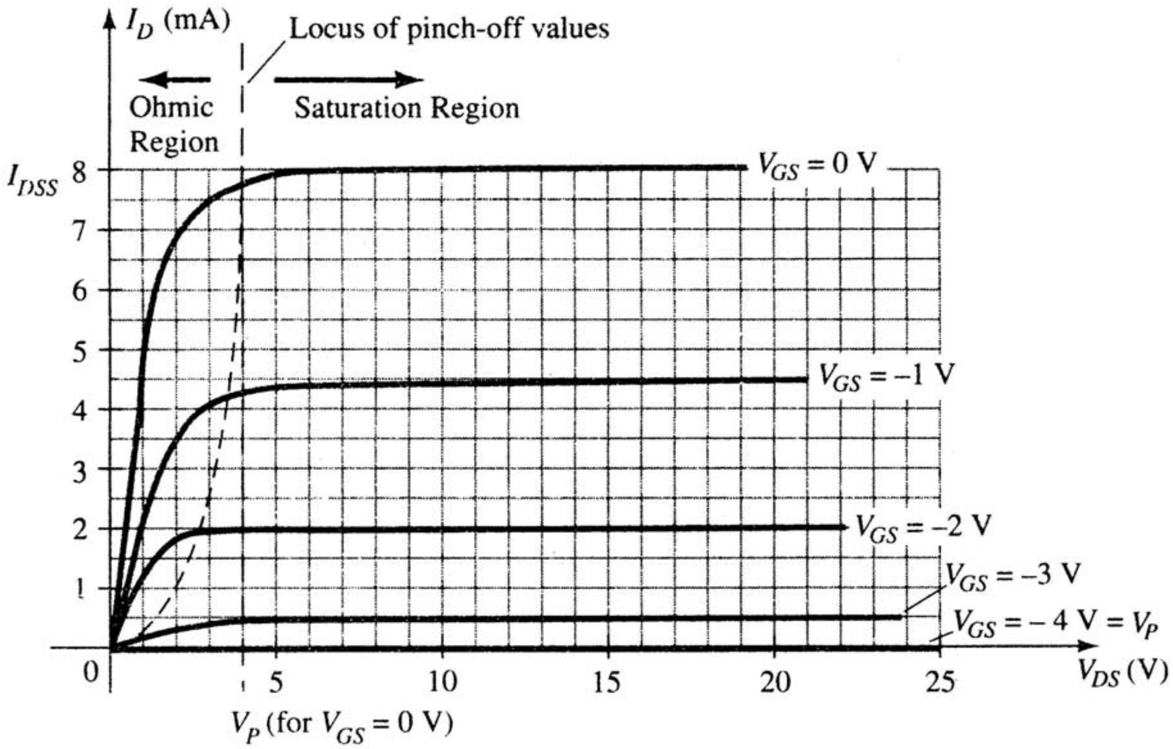


Junction Field Effect Transistors - JFET

Level of V_{GS} when $I_D = 0$ is defined as V_P

V_P is negative for *n*-channel and positive for *p*- channel

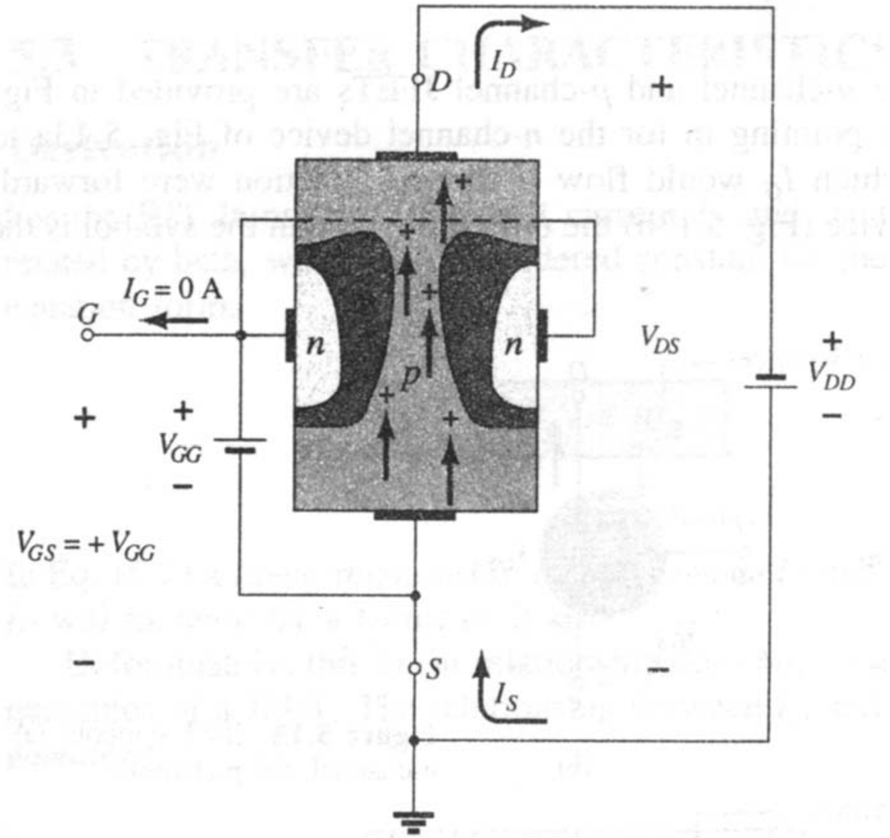
Region left of locus of pinch off values is called as ohmic or voltage controlled resistance (V_{DS}). Possible use in automatic gain control, where resistance can be controlled by voltage.



Junction Field Effect Transistors - JFET

p-channel type

Behaves exactly same as *n*-channel type. Current direction and the polarities for V_{GS} and V_{DS} changes. V_{GS} is positive and this will create more reverse bias.



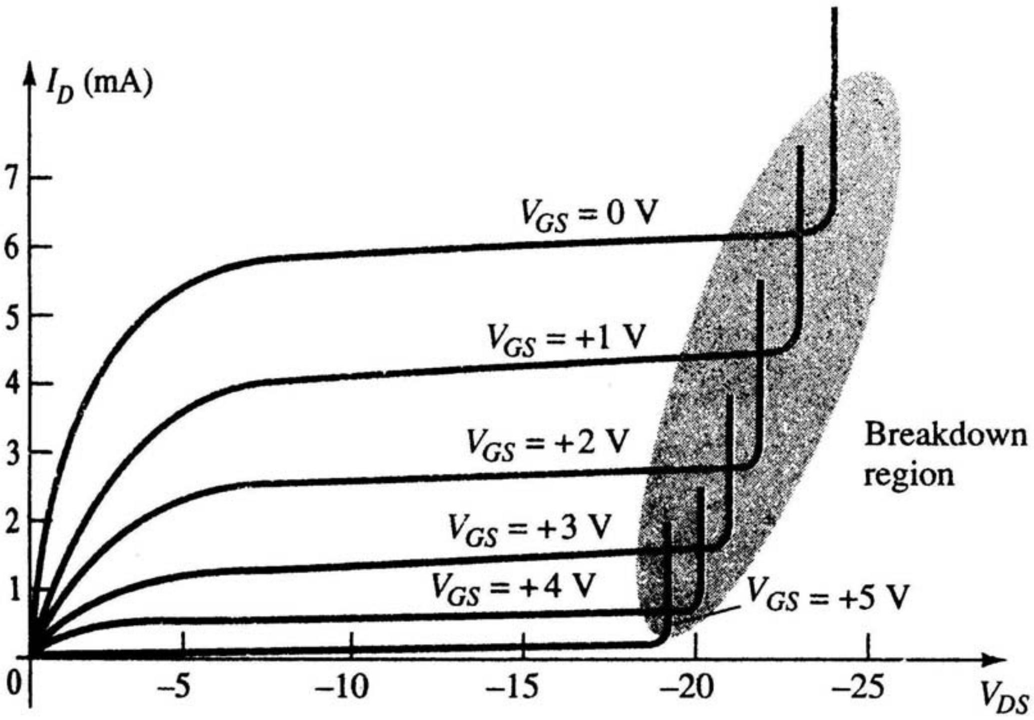
p-Channel JFET.

Junction Field Effect Transistors - JFET

p-channel type, characteristics

$V_P > 0$

Current is unbounded in the breakdown region. This will damage the transistor.



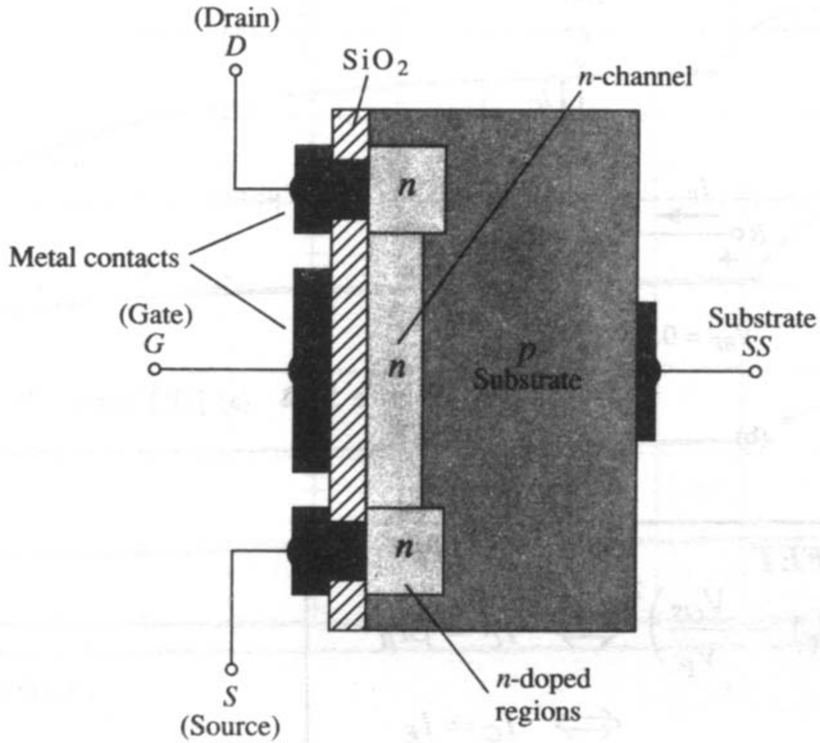
Metal Oxide Semiconductor Field Effect Transistors - MOSFET

n-type channel is constructed over a *p*-type substrate in form of slab

Many times substrate and source are connected internally and it is a three terminal device

Source and drain are connected at each end of *n*-channel

Gate and *n*-channel are separated by insulator SiO_2 layer (dielectric)

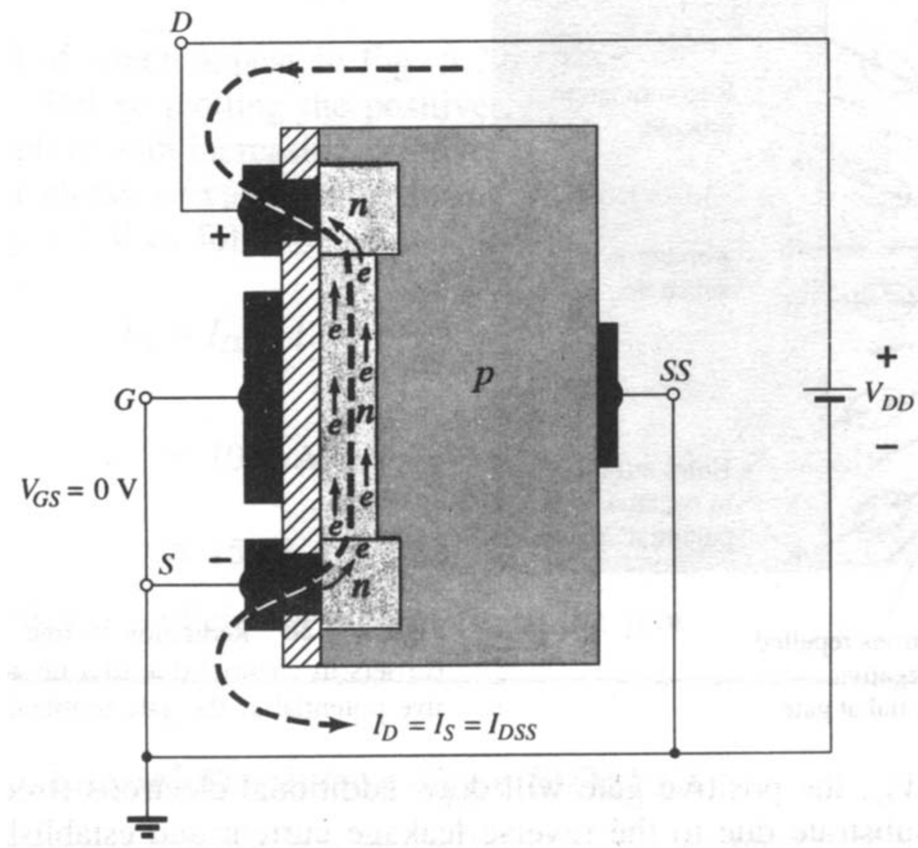


Depletion type MOSFET-Basic operation

V_{GS} = 0v, V_{DS} > 0

Operation similar to JFET

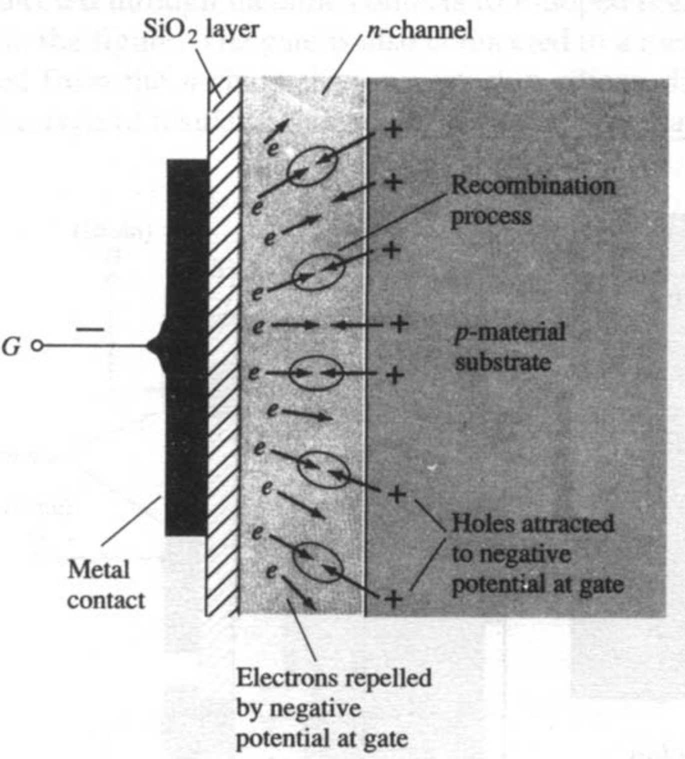
Current flows through *n*-channel. Free electrons are attracted to positive terminal of drain. Channel ohmic resistance is offered.

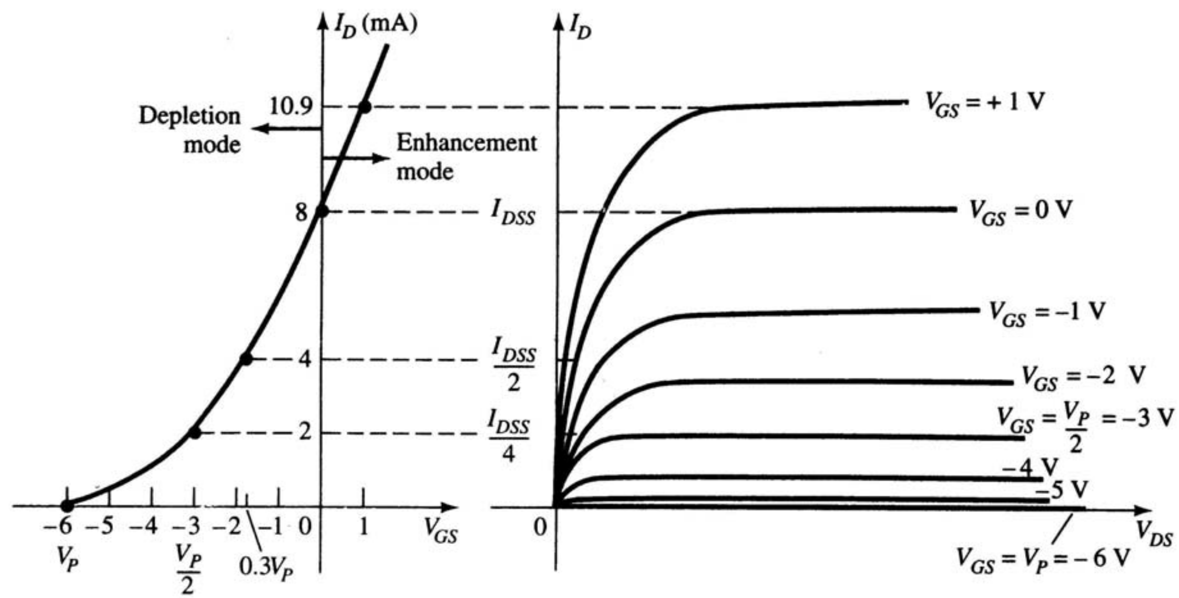


Depletion type MOSFET-Basic operation

When V_{GS} is negative, the electric field will pressure electrons towards *p*-type substrate, hence reduce free carrier in *n*-channel or depleting the majority carrier

When V_{GS} is positive it enhances the current. It is limited by the maximum current capacity of the device





Drain and transfer characteristics for an *n*-channel depletion-type MOSFET.

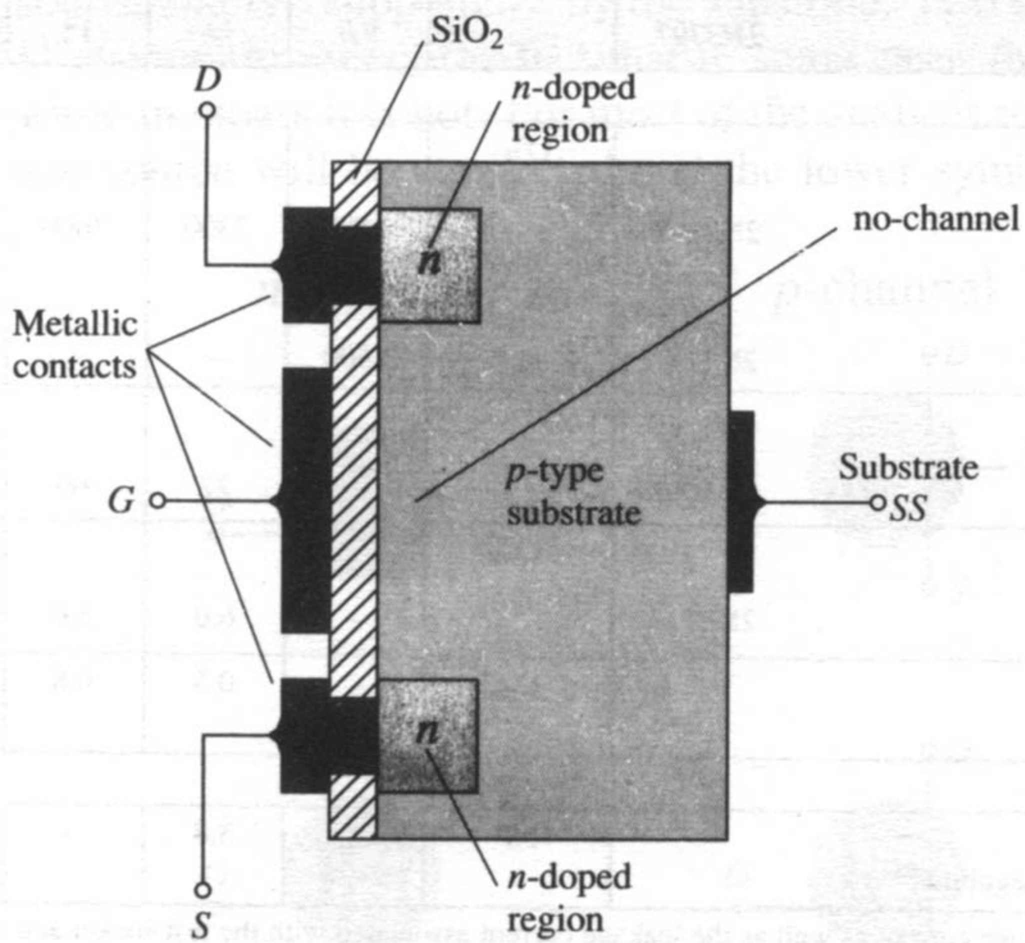
Enhancement type MOSFET

p-type substrate in form of slab with no *n*-channel

Many times substrate and source are connected internally and it is a three terminal device

Source and drain are connected to two *n*-doped region

Gate and *p*-substrate are separated by insulator SiO_2 layer (dielectric)

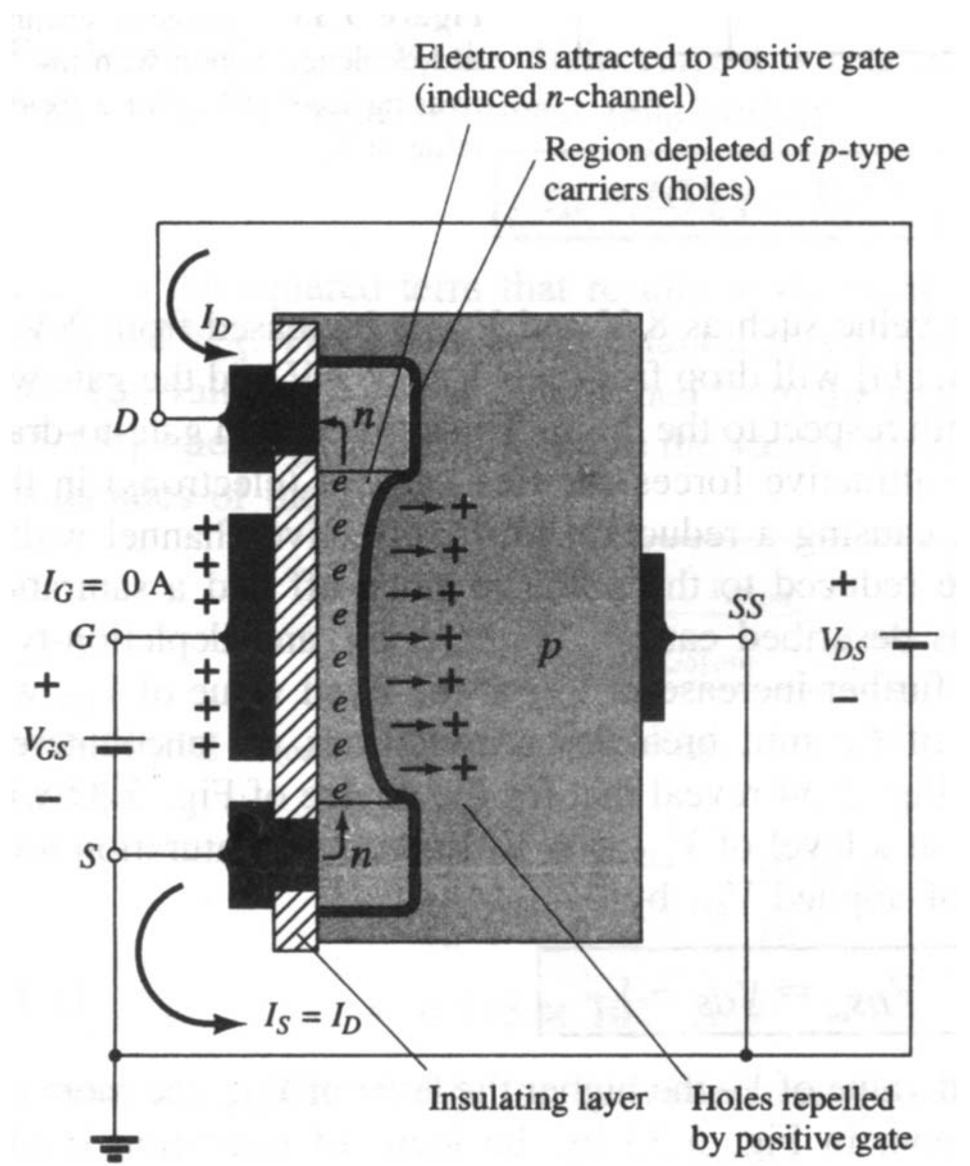


Enhancement type MOSFET

When $V_{GS} = 0$ and $V_{DS} > 0$

No link between two *n*-doped region and hence no current

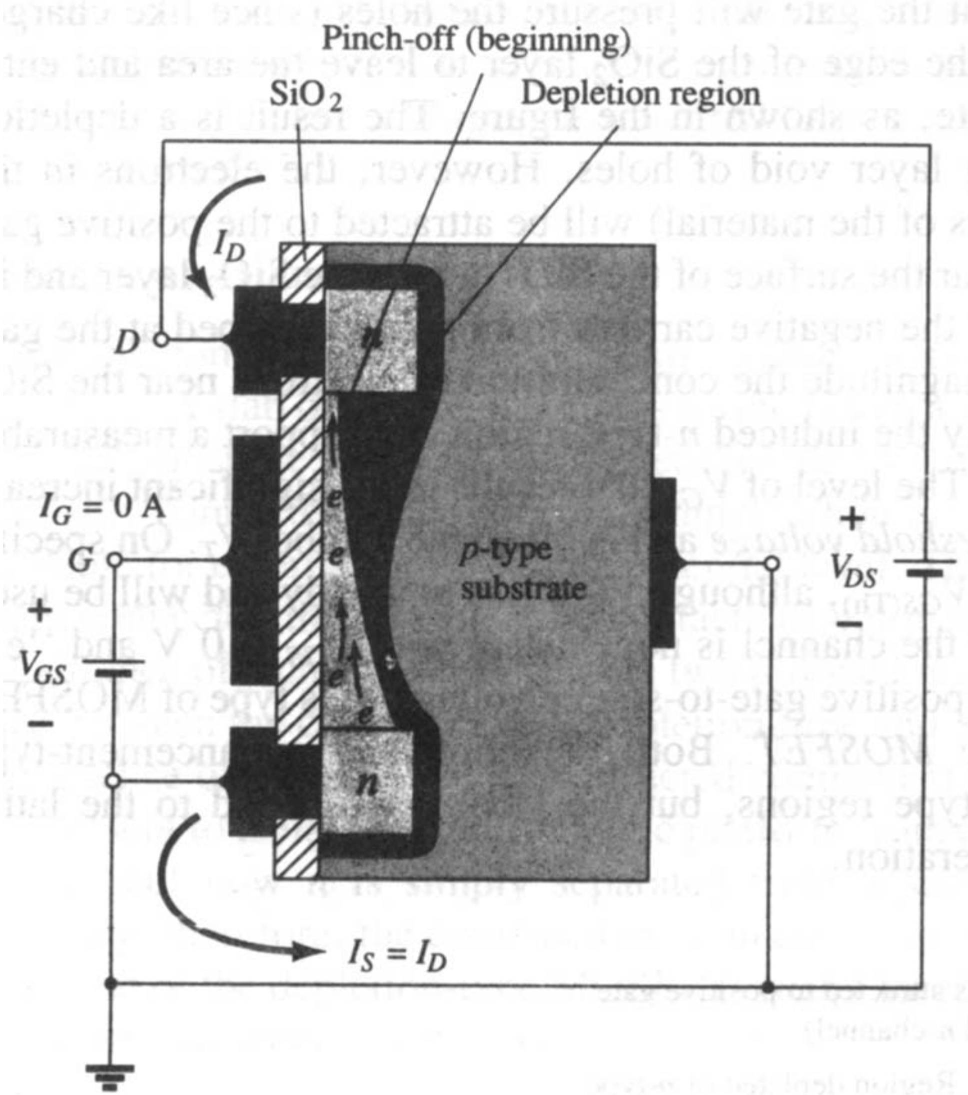
V_{GS} and $V_{DS} > 0$ This will push the holes away from the SiO_2 edge and attracts electrons from the *p*-substrate. When sufficient voltage is applied it creates a *n*-channel, this is called threshold voltage V_T



Enhancement type MOSFET

If V_{GS} is increased beyond threshold voltage, I_D will increase.

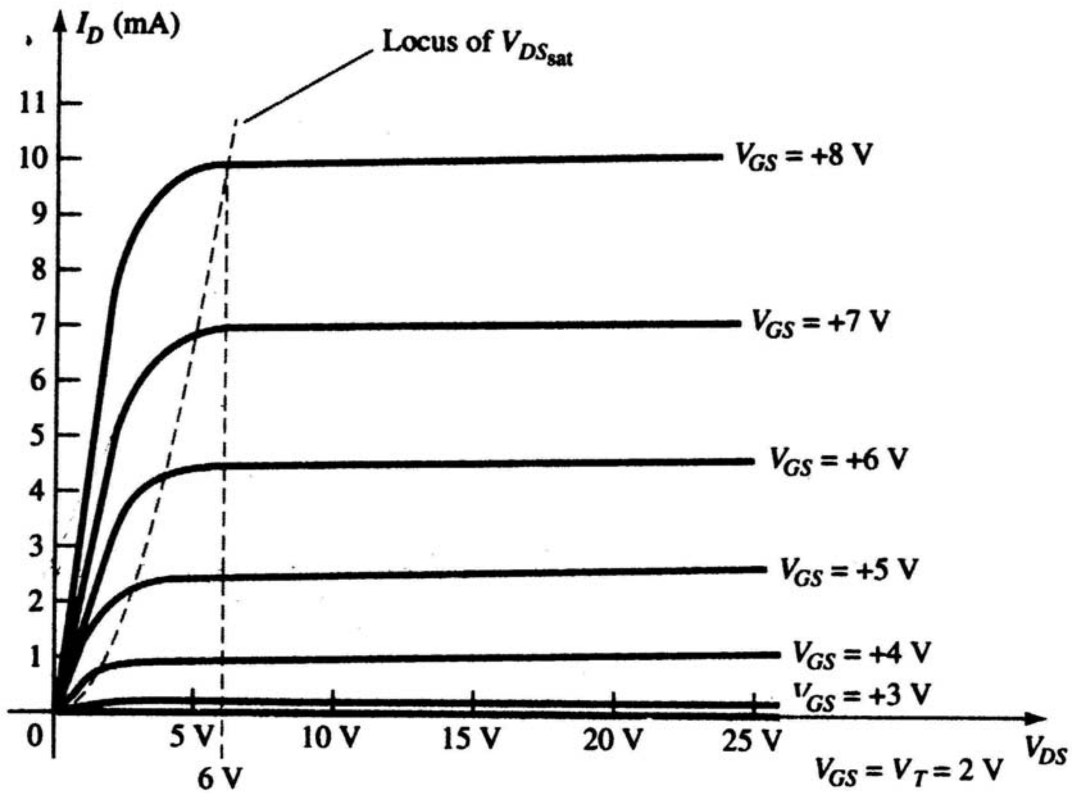
If V_{GS} is kept constant beyond threshold voltage, and V_{DS} is increased then I_D will reach saturation level similar to JFET (pinch off)



Enhancement type MOSFET

Values less than threshold value I_D is zero

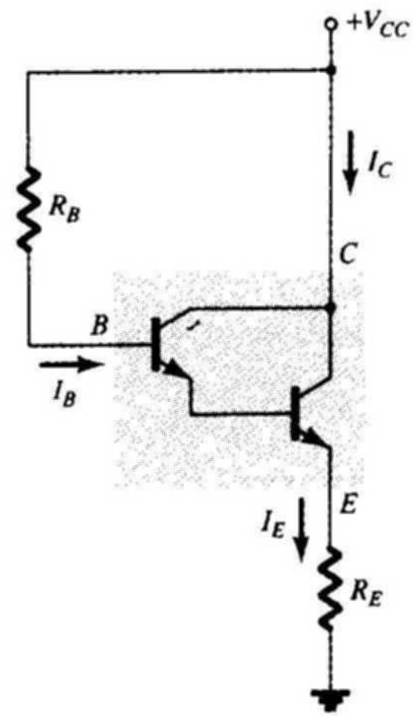
V_{GS} increases V_{DSsat}



Drain characteristics of an *n*-channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.278 \times 10^{-3}$ A/V^2.

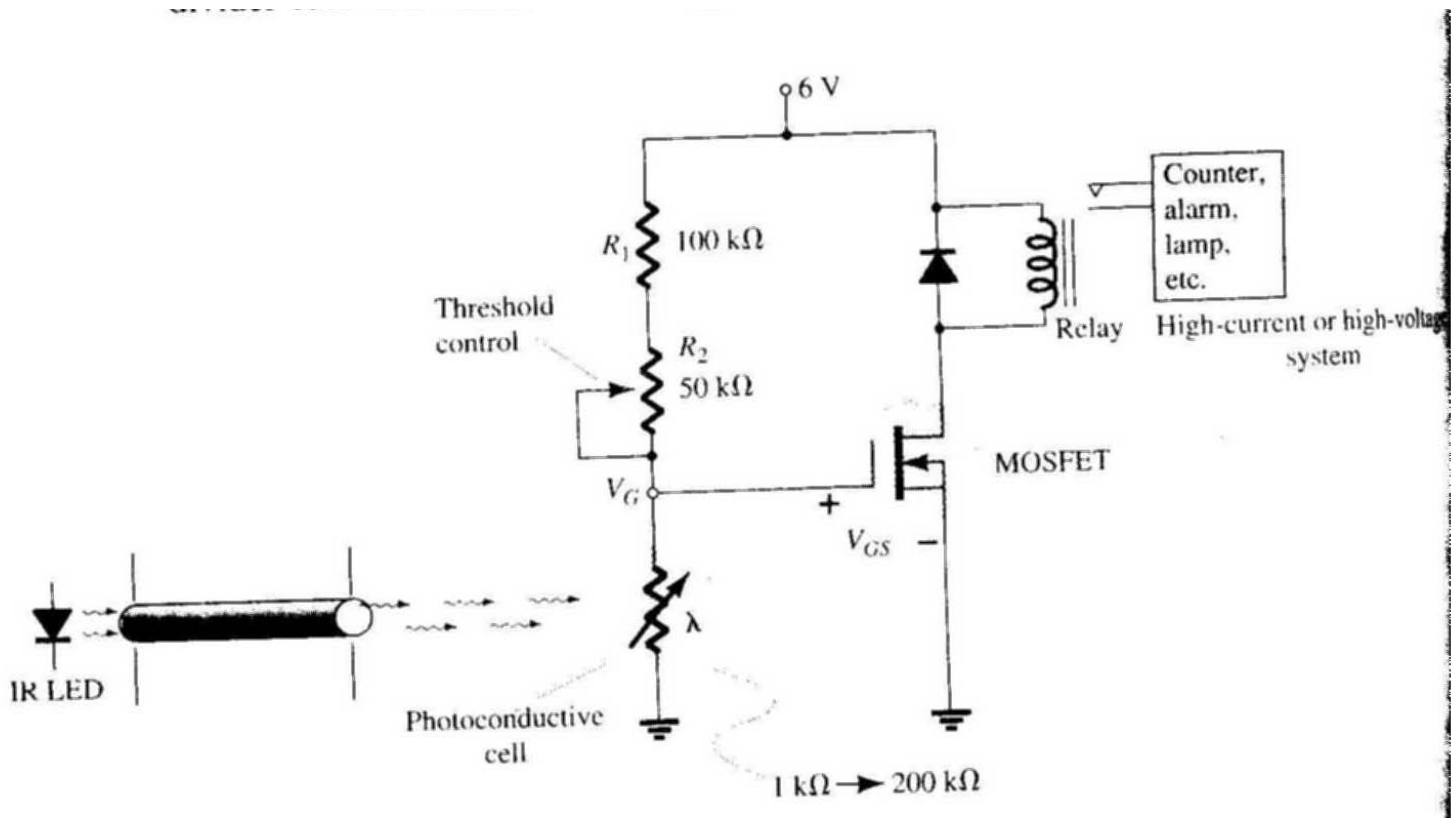
Darlington Pair circuit

Used as high current current component. Current amplification of the order of β^2 Can be easily integrated with microcontroller for interfacing DC motor, relays etc.



MOSFET as relay driver

When photodiode not conducting Gate is positive and no current in MOSFET. When photodiode is conducting Gate is grounded and current is passed through MOSFET.



BJT and UJT

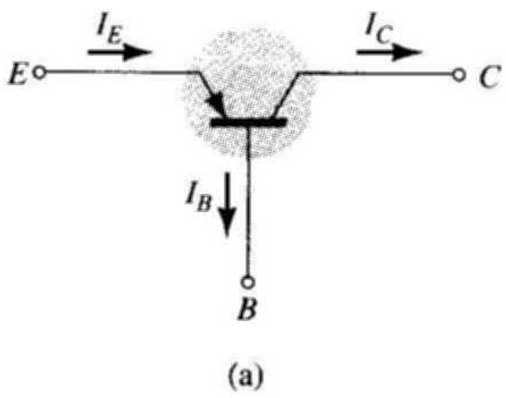
BJT - Current controlled devices

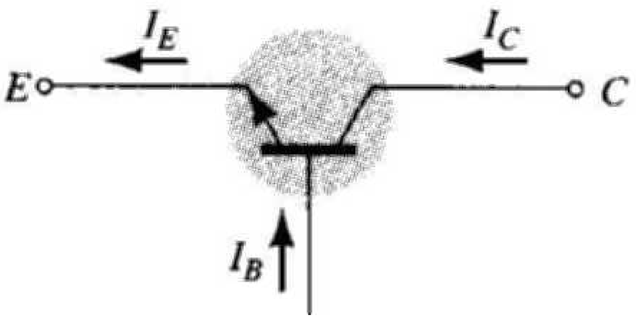
- electron & holes participate in conduction
- Robust in handling

UJT - Voltage controlled devices

- Only one type of carrier participate in conduction
- Smaller in size and more devices can be packed
- Sensitive to static charge (MOSFET)
- Very high input impedance
- Less noisy

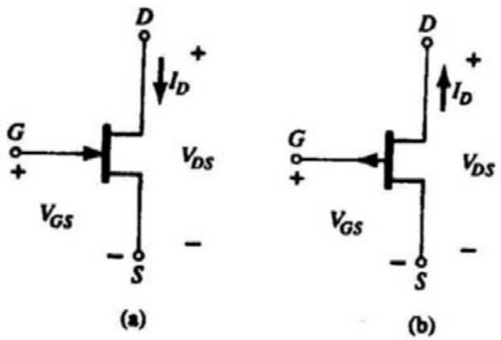
BJT symbols

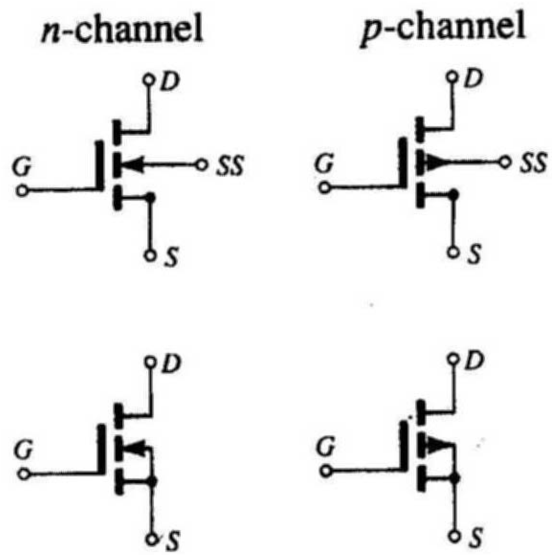


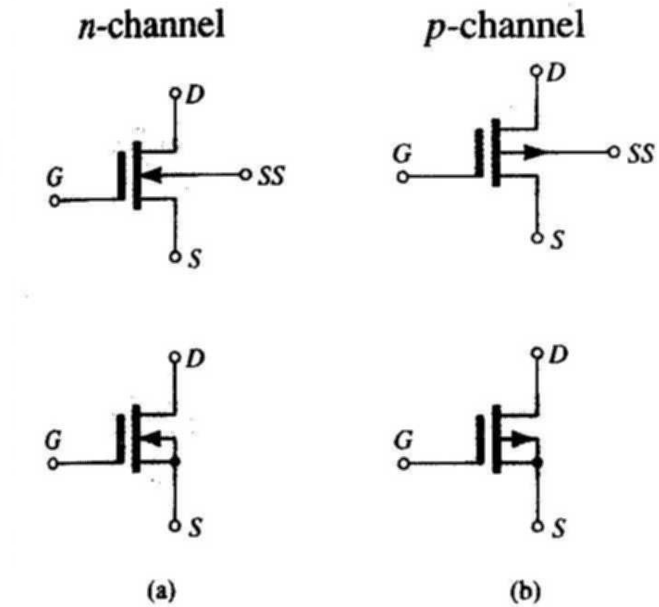


BJT a) *pnp* b) *npn*

UJT symbols







JFET a) *n*- channel

b) *p*- channel

MOSFET enhancement

a) *n*- channel

b) *p*- channel

MOSFET depletion

a) *n*- channel

b) *p*- channel